12.6V, 7A Fully Integrated High Efficiency Synchronous Boost Converter

FEATURES

- Wide Input Voltage Range: 2.7V-12V
- Wide Output Voltage Range: 4.5V-12.6V
- Fully Integrated 17mΩ High Side FET and 14mΩ Low Side FET
- Up to 93% Efficiency at Vin=3.3V, Vout=9V, and Iout=2A
- Programmable and Up to 9.5A Peak Switch Current Limit
- Typical Shut-down Current: 1uA
- Quiescent Current: 150uA
- Adjustable Switching Frequency: 200KHz to 2.2MHz
- PFM Operation Mode at Light Load
- Internal Soft Start and External Compensation
- Cycle-by-Cycle Overcurrent Protection
- Output Overvoltage Protection
- Thermal Shutdown Protection: 160°C
- QFN-11 2mm x 2.5mm Package

APPLICATIONS

- Bluetooth Speaker
- Portable POS Terminal
- Quick Charge Power Bank
- E-Cigarette
- Outdoor Flashlight

DESCRIPTION

The SCT1271 is a high efficiency synchronous boost converter with fully integrated a 17mΩ high-side MOSFET and a 14mΩ low-side MOSFET, featuring 2.7V to 12V input voltage range to support single cell or two cell Lithium ion/polymer batteries and up to 9.5A peak switch current. The switch current limit can be adjustable with an external resistor. The SCT1271 has 7A continuous switch current capability and provides output voltage up to 12.6V.

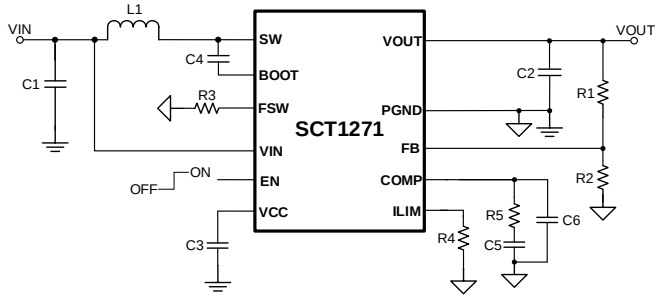
The SCT1271 adopts constant off-time peak current control to provide fast transient response. An external compensation network allows flexibility setting loop dynamics to achieve optimal transient performance at different load conditions.

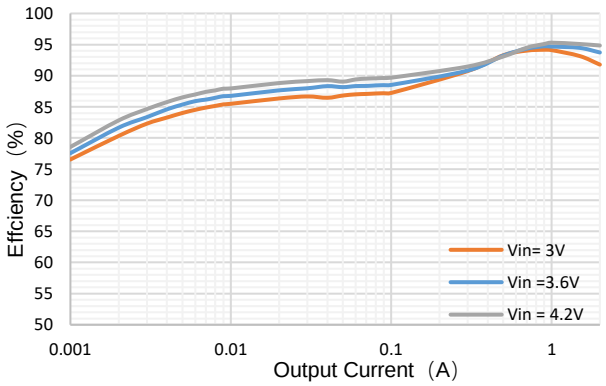
The SCT1271 works in the PWM at moderate and heavy load condition. The SCT1271 offers PFM mode at light load condition. The switching frequency is adjustable from 200KHz to 2.2MHz.

The SCT1271 features output overvoltage protection and thermal shutdown protection when the device over loads.

The device is available in a QFN-11 2mm x 2.5mm package.

TYPICAL APPLICATION





Efficiency vs Load Current, Vout=9V

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production

Revision 1.1: Update T_J to 150 ºC

Revision 1.2: Update Equation 3

Revision 1.3: Update DEVICE ORDER INFORMATION

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT1271FQAR	Tape & Reel	3000	1271	11	11-Lead 2mm×2.5mm Plastic QFN

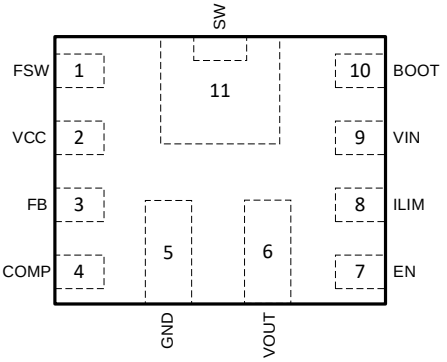
ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
BOOT	-0.3	21.5	V
VIN, SW, FSW, VOUT	-0.3	14.5	V
VCC, LIM, FB, EN, COMP, MODE	-0.3	5.5	V
BOOT-SW	-0.3	5.5	V
Operating ambient temperature T_A	-40	125	°C
Operating junction temperature T_J(2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION

Top View: 11-Lead Plastic QFN 2mm x 2.5mm



(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
FSW	1	Place a resistor from this pin to GND to sets the switching frequency.
VCC	2	Internal linear regulator output. Connect a 1uF or larger ceramic capacitor to ground. VCC can not to be externally driven. No additional components or loading is recommended on this pin.
FB	3	Feedback Input. Connect a resistor divider from VOUT to FB to set up output voltage.
COMP	4	Output of the error amplifier and switching converter loop compensation point.
GND	5	Ground
VOUT	6	Boost converter output. Connect a 1uF decoupling capacitor as close to VOUT pins and power ground pad as possible to reduce the ringing voltage of SW.
EN	7	Enable logic input. An 750KΩ resistor connects this pin to ground inside. Floating disables the device.
ILIM	8	Inductor peak current limit set point input. A resistor connecting this pin to ground sets current limit through low-side power FET.

VIN	9	Power supply input. Must be locally bypassed with a capacitor as close as possible to the pin.
BOOT	10	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BOOT pin and SW node.
SW	11	Switching node of the boost converter.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	2.7	12	V
V_{OUT}	Output voltage range	4.5	12.6	V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(2)	-0.5	+0.5	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	QFN-11L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	53.4	°C/W
$R_{\theta JC}$	Junction to case thermal resistance(1)	59.2	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT1271 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT1271. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN}=3.6V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.7		12	V
V_{OUT}	Output voltage range		4.5		12.6	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		2.5 200		V mV
I_{SD}	Shutdown current	EN=0, no load and measured on VIN pin		1		uA
I_Q	Quiescent current from VIN	EN=2V, no load, no switching		1.8		uA
	Quiescent current from VOUT			150		uA
V_{CC}	Internal linear regulator	I_{VCC}=5mA, V_{IN}=6V		4.75		V
V_{CC_UVLO}	VCC UVLO threshold	V_{IN} falling		2.2		V
Reference and Control Loop						
V_{REF}	Reference voltage of FB		0.98	1	1.02	V
I_{FB}	FB pin leakage current	V_{FB}=1V			100	nA
G_{EA}	Error amplifier trans-conductance	V_{COMP}=1.5V		200		uS
I_{COMP_SRC}	Error amplifier maximum source current	V_{FB}=V_{REF}-200mV, V_{COMP}=1.5V		24		uA
I_{COMP_SNK}	Error amplifier maximum sink current	V_{FB}=V_{REF}+200mV, V_{COMP}=1.5V		24		uA
V_{COMP_H}	COMP high clamp	V_{FB}=0.8V, R_{ILIM}=100kΩ		2.2		V
V_{COMP_L}	COMP low clamp	V_{FB}=1.2V, R_{ILIM}=100kΩ, PFM		0.9		V
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			17		mΩ
R_{DSON_L}	Low side FET on-resistance			14		mΩ
Current Limit						
I_{LIM}	Peak current limit	R_{ILIM}=100kΩ	7.2	8	8.8	A
		R_{ILIM}=84kΩ		9.5		A
Enable						
V_{EN}	Enable high threshold Enable low threshold		 0.4		1.2	V V
R_{EN}	Enable pull down resistance			750		kΩ
T_{SS}	Soft-start Current			4		ms
Switching Frequency						
F_{SW}	Switching frequency	R_{FSW}=259kΩ, V_{OUT}=12V		500		kHz
t_{ON_MIN}	Minimum on-time	R_{FSW}=259kΩ, V_{OUT}=12V		170		ns
Protection						
V_{OVP_VOUT}	Output overvoltage threshold Hysteresis	V_{OUT} rising		13.2 280		V mV
T_{SD}	Thermal shutdown threshold*	T_J rising		164		°C
	Hysteresis*			24		°C

*Derived from bench characterization

TYPICAL CHARACTERISTICS

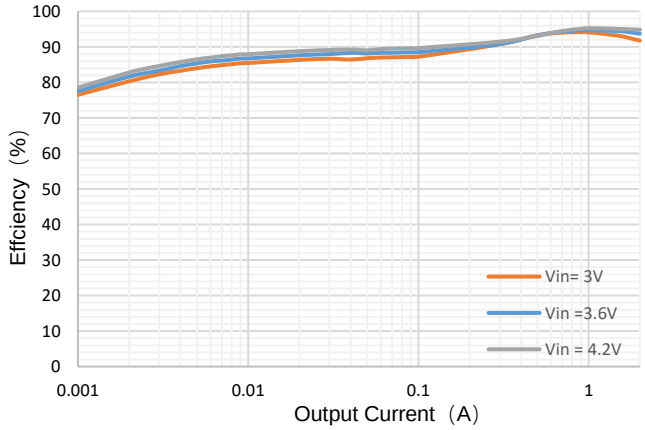


Figure 1. SCT1271 Efficiency vs Load Current, Vout=9V

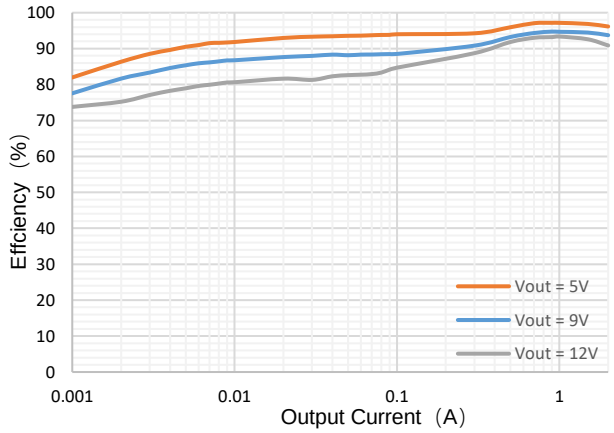


Figure 2. SCT1271 Efficiency vs Load Current, Vin=3.6V

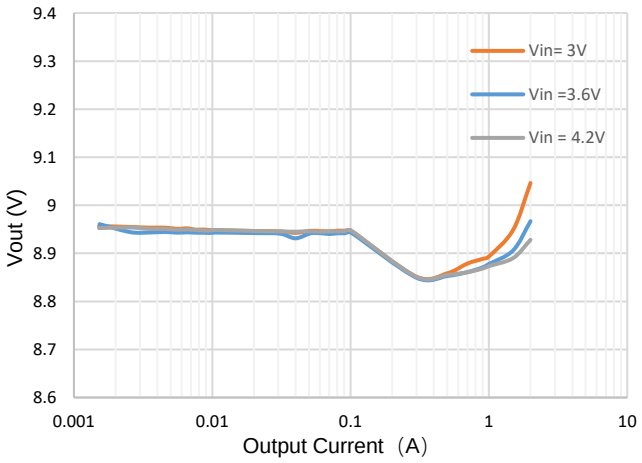


Figure 3. Load Regulation (Vin=3.6V, Vout=9V)

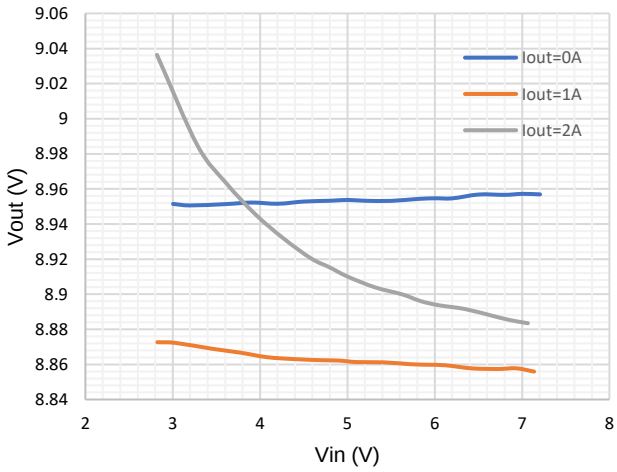


Figure 4. Line Regulation, Vout=9V

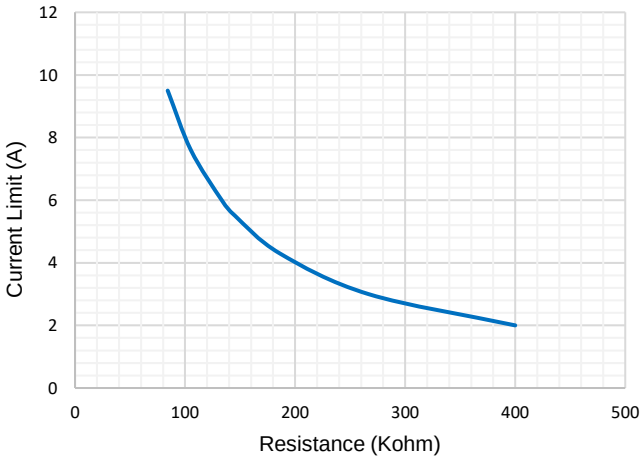


Figure 5. Current Limit VS Setting Resistance

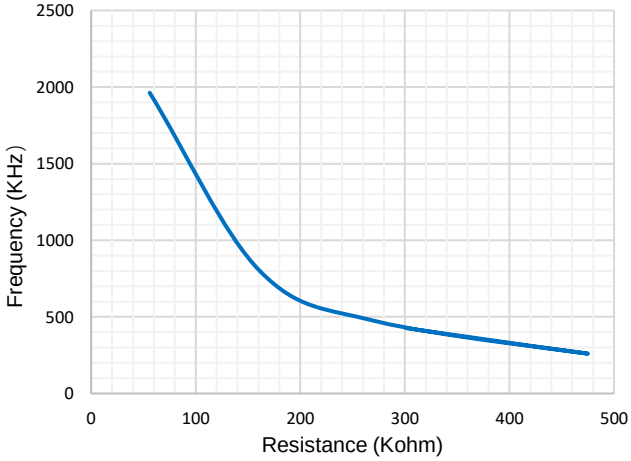


Figure 6. Switching Frequency VS Setting Resistance

FUNCTIONAL BLOCK DIAGRAM

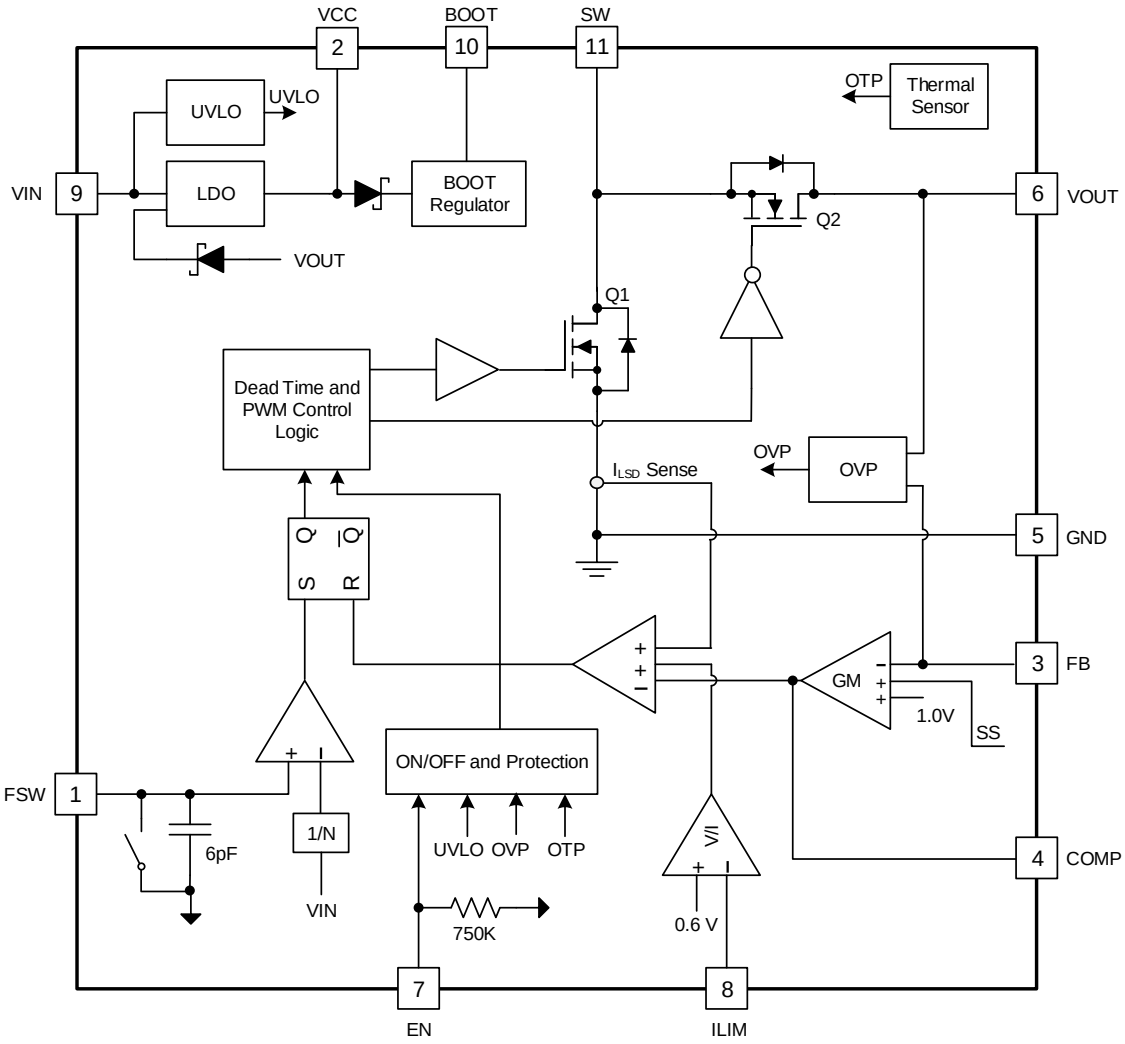


Figure 7. Functional Block Diagram

OPERATION

Overview

The SCT1271 device is a fully integrated synchronous boost converter, which regulates output voltage higher than input voltage. The constant off-time peak current mode control provides fast transient with pseudo fixed switching frequency. When low-side MOSFET Q1 turns on, input voltage forces the inductor current rise. Sensed voltage on low-side MOSFET peak current rises above the voltage determined by COMP. After the inductor current reaches the peak current, the device turns off low-side MOSFET and inductor goes through body diode of high-side MOSFET Q2 during dead time. After dead time duration, the device turns on high-side MOSFET Q2 and the inductor current decreases. Based on Vin and Vout voltage, the device predicts required off-time and turns off high-side MOSFET Q2. This repeats on cycle-by-cycle based.

The voltage feedback loop regulates the FB voltage to an internal voltage reference with an integrated trans-conductance error amplifier. The feedback loop stability and transient response are optimized through an external loop compensation network connected to the COMP pin.

The SCT1271 works at PFM mode to further increase the efficiency in light load condition. The quiescent current of SCT1271 is 150uA typical under no-load condition and not switching. Disabling the device, the typical supply shutdown current on VIN pin is 1μA.

A resistor connected between SW pin and the FSW pin sets the switching frequency. The wide switching frequency range of 200 kHz to 2.2 MHz offers optimization on efficiency or size of filter components.

The SCT1271 device features internal soft-start, cycle-by-cycle low-side FET current limit, over-voltage protection, and over-temperature protection.

The SCT1271 uses the thermal pad as the power ground. Power ground must be connected to the thermal pad on the PCB at the closest point.

VIN Power

The SCT1271 is designed to operate from an input voltage supply range between 2.7 V to 12V. If the input supply is located more than a few inches from the converter, additional bulk capacitance is required in addition to the ceramic bypass capacitors. A typical choice is ceramic capacitor with a value of 47μF or 2 x 22uF.

VCC Power

The internal VCC LDO provides the bias power supply for internal circuitries. A ceramic capacitor of no less than 1uF is required to bypass from VCC pin to ground. During starting up, input of VCC LDO is from VIN pin. Once the output voltage at VOUT pin exceeds VIN voltage, VCC LDO switches its input to VOUT pin. This allows higher voltage headroom of VCC at lower input voltage. The maximum current capability of VCC LDO is 130mA typical. No additional components or loading are recommended on this pin.

Under Voltage Lockout UVLO

The SCT1271 features UVLO protection for voltage rails of VIN, VCC and BOOT-SW from the converter malfunctioning and the battery over discharging. The default VIN rising threshold is 2.5V typical at startup and falling threshold is 2.3V typical at shutdown. The internal VCC LDO dropout voltage is about 100mV and the device is disabled when VCC falling trips 2.2V typical threshold. The internal charge pump from BOOT to SW powers the gate driver to high-side MOSFET Q2. The BOOT UVLO circuit monitors the capacitor voltage between BOOT pin and SW pin. When the voltage of BOOT to SW falls below a preset threshold 3V typical, high-side MOSFET Q2 turns off. As a result, the device works as a non-synchronous boost converter.

Enable and Start-up

When applying a voltage higher than the EN high threshold (maximum 1.2V), the SCT1271 enables all functions and starts converter operation. To disable converter operation, EN voltage needs fall below its lower threshold

(minimum 0.4V). An internal 750KΩ resistor connects EN pin to the ground. Floating EN pin automatically disables the device.

The SCT1271 features fixed 4ms soft start to prevent inrush current during power-up.

Adjustable Peak Current Limit

The SCT1271 boost converter implements cycle-by-cycle peak current limit function with sensing the internal low-side power MOSFET Q1 during overcurrent condition. While the Q1 is turned on, its conduction current is monitored by the internal sensing circuitry. Once the low-side MOSFET Q1 current exceeds the limit, it turns off immediately. An external resistor connecting ILIM pin to ground sets the low-side MOSFET Q1 peak current limit threshold. Use Equation 1 or Figure 5 to calculate the peak current limit.

$$I_{LIM}(A) = \frac{800}{R_{LIM}(k\Omega)} \quad (1)$$

where:

- I_{LIM} is the peak current limit
- R_{LIM} is the resistance between ILIM pin to ground.

This current limit function is realized by detecting the current flowing through the low-side MOSFET. The current limit feature loses function in the output hard short circuit conditions. At normal operation, when the output hard shorts to ground, there is a direct path to short the input voltage through high-side MOSFET Q2 or its body diode even the Q2 is turned off. This could damage the circuit components and cause catastrophic failure at load circuit.

Adjustable Switching Frequency

The SCT1271 features a wide adjustable switching frequency ranging from 200kHz to 2.2MHz. The switching frequency is set by a resistor connected between the FSW pin and the GND pin of SCT1271. Do not leave the FSW pin open. Use Equation 2 to calculate the resistor value required for a desired frequency.

$$R_{FREQ} = \frac{\frac{1}{f_{SW}-70K} - T_{DELAY} * \frac{V_{OUT}}{V_{IN}}}{C_{FREQ}} \quad (2)$$

where:

- f_{SW} is the desired switching frequency
- T_{DELAY} = 70 ns
- C_{FREQ} = 6 pF
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

Over Voltage Protection and Minimum On-time

The SCT1271 features VOUT pin over voltage protection. If the VOUT pin is above 13.2V typical, the device stops switching immediately until the VOUT pin drops below 12.92V. The OVP function prevents the connected output circuitry from un-predictive overvoltage.

The low-side MOSFET has minimum on-time 170ns typical limitation. While the device is operating at minimum on time and further increasing Vin push output voltage beyond regulation point. With output and feedback over voltage protection, the converter skips pulse with turning off high-side MOSFET and prevents output running higher to damage the load.

PFM Mode

The SCT1271 improves the efficiency at light load with the PFM mode. When the converter operates in light load condition, the output of the internal error amplifier decreases to make the inductor peak current down, delivering less power to the load. When the output current further reduces, the current through the inductor will decrease to zero during the off-time. Once the current through the high side N-MOSFET is zero, the high-side MOSFET is turned off until the beginning of the next switching cycle. When the output of the error amplifier continuously goes down

and reaches a threshold with respect to the peak current of I_{LIM} / 10, the output of the error amplifier is clamped at this value and does not decrease any more. If the load current is smaller than what the SCT1271 delivers, the output voltage increases above the nominal setting output voltage. The SCT1271 extends its off time of the switching period to deliver less energy to the output and regulate the output voltage to 1.0% higher than the nominal setting voltage. With the PFM operation mode, the SCT1271 keeps the efficiency above 70% even when the load current decreases to 1 mA. At light load, the output voltage ripple is much smaller due to low peak inductor current. Refer to Figure 17.

Thermal Shutdown

Once the junction temperature in the SCT1271 exceeds 164 ^{O}C, the thermal sensing circuit stops switching until the junction temperature falling below 140 ^{O}C, and the device restarts. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

APPLICATION INFORMATION

Typical Application

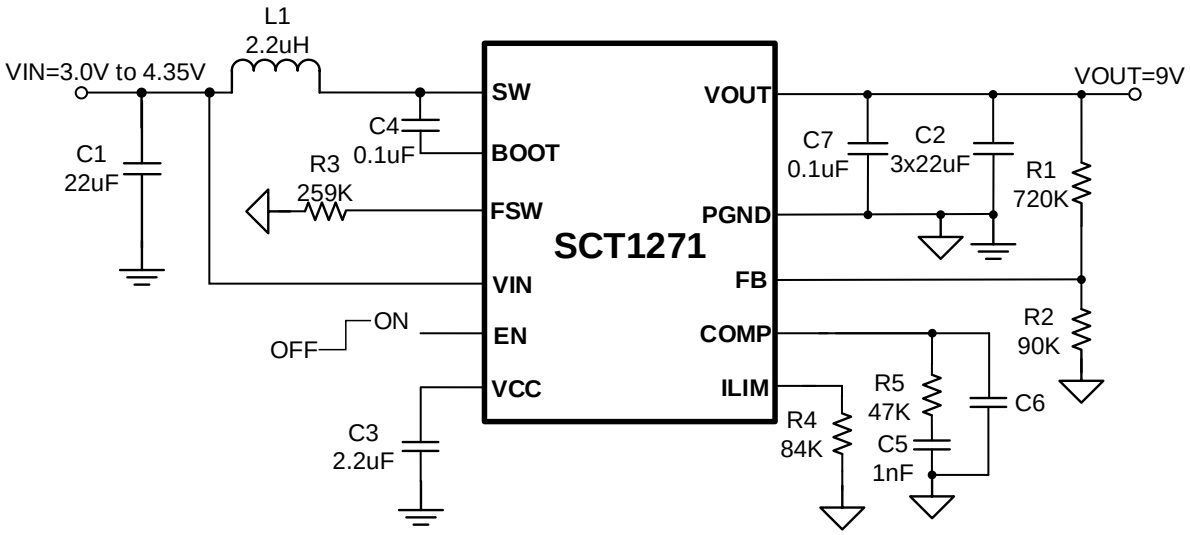


Figure 8. One Cell Battery Input, 9V/2A (20W) Output

Design Parameters

Design Parameters	Example Value
Input Voltage	3.0V to 4.35V
Output Voltage	9V
Output Current	2A
Output voltage ripple (peak to peak)	100mV
Switching Frequency	500 kHz
Operation Mode	PFM

Switching Frequency

The resistor connected from FSW to GND sets switching frequency of the converter. The resistor value required for a desired frequency can be calculated using equation 3. High frequency can reduce the inductor and output capacitor size with the tradeoff of more thermal dissipation and lower efficiency.

$$R_{FREQ} = \frac{\frac{1}{f_{SW}+70K} - T_{DELAY} * \frac{V_{OUT}}{V_{IN}}}{C_{FREQ}} \quad (3)$$

where:

- f_{SW} is the desired switching frequency
- T_{DELAY} = 70 ns
- C_{FREQ} = 6 pF
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

Table 1. R_{FSW} Value for Common Switching Frequencies (Vin=3.6V, Vout=9V, Room Temperature)

Fsw	R_{FREQ}
200 KHz	590 KΩ
370 KHz	350 KΩ
560 KHz	235 KΩ
860 KHz	150 KΩ
1000 KHz	126 KΩ
2000 KHz	51 KΩ

Peak Current Limit

Using the correct external resistor at ILIM pin sets the peak input current. Table 2 shows the resistor value for inductor peak current limit. For a typical current limit of 9.5A, the resistor value is 84KΩ. The minimum current limit must be higher than the required peak switch current at lowest input voltage and the highest output power not to hit the current limit and still regulate the output voltage.

$$I_{LIM}(A) = \frac{800}{R_{LIM}(k\Omega)} \quad (4)$$

where:

- I_{LIM} is the peak current limit
- R_{LIM} is the resistance of ILIM pin to ground

Table 2. R_{LIM} Value for Inductor Peak Current (Vin=3.6V, Vout=9V, L=2.2uH, Room Temperature)

I_{LIM}	R_{LIM}
9.5 A	84 KΩ
8 A	100 KΩ
5.6A	142 KΩ
4A	200 KΩ

Output Voltage

The output voltage is set by an external resistor divider R3 and R4 in typical application schematic. A minimum current of typical 20uA flowing through feedback resistor divider gives good accuracy and noise covering. The value of R3 can be calculated by equation 5.

$$R_1 = \frac{(V_{OUT} - V_{REF}) \times R_2}{V_{REF}} \quad (5)$$

where:

- V_{REF} is the feedback reference voltage, typical 1.0V

Table 3. Feedback Resistor R_1 R_2Value for Output Voltage (Room Temperature)

V_{OUT}	R_1	R_2
5 V	360 KΩ	90 KΩ
9 V	720 KΩ	90 KΩ
12 V	990 KΩ	90 KΩ

Inductor Selection

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and boost converter efficiency. The inductor value, DC resistance, and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DC resistance, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a boost converter, calculate the inductor DC current as in equation 6

$$I_{LDC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (6)$$

Where

- V_{OUT} is the output voltage of the boost converter
- I_{OUT} is the output current of the boost converter
- V_{IN} is the input voltage of the boost converter
- η is the power conversion efficiency

Calculate the inductor current peak-to-peak ripple, I_{LPP}, as in equation 7

$$I_{LPP} = \frac{1}{L \times (\frac{1}{V_{OUT}-V_{IN}} + \frac{1}{V_{IN}}) \times f_{SW}} \quad (7)$$

Where

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Therefore, the peak switching current of inductor, I_{LPEAK}, is calculated as in equation 8.

$$I_{LPEAK} = I_{LDC} + \frac{I_{LPP}}{2} \quad (8)$$

Set the current limit of the SCT1271 higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit.

The inductor's DC resistance (DCR) and the core loss significantly affect the efficiency of power conversion. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss. Usually, a data sheet of an inductor does not provide the ESR and core loss information. If needed, consult the inductor vendor for detailed information. There is a tradeoff among the inductor's inductance, DCR and ESR resistance, and its footprint. Shielded inductors typically have higher DCR than unshielded inductors. Table 4 lists recommended inductors for the SCT1271. Verify whether the recommended inductor can support the user's target application with the previous

calculations and bench evaluation. In this application, the Wurth-Elektronix 's inductor 744313220 is used on SCT1271 evaluation board.

Table 4. Recommended Inductors

Part Number	L (uH)	DCR Max (mΩ)	Saturation Current/Heat Rating Current (A)	Size Max (LxWxH mm)	Vendor
744325180	1.8	3.5	18 / 14	10.5 x 10.2 x 4.7	Wurth Elektronix
744311150	1.5	7.2	14 / 11	7.3 x 7.2 x 4.0	Wurth Elektronix
744311220	2.2	12.5	13 / 9	7.3 x 7.2 x 4.0	Wurth Elektronix
744313220	2.2	5.7	18 / 14	12.9 x 12.8 x 3.3	Wurth Elektronix
CDMC8D28NP-1R8MC	1.8	12.6	9.4 / 9.3	9.5 x 8.7 x 3.0	Sumida

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT1271. A ceramic capacitor of more than 1.0μF is required at the VCC pin to get a stable operation of the internal LDO.

For the power stage, because of the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the inductor. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, 2x 22μF input capacitance is recommended for most applications. Choose the right capacitor value carefully by considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Output Capacitor Selection

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor. Typically, three 22μF ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. Due to a capacitor's derating under DC bias, the bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. From the required output voltage ripple, use the equation 9 and 10 to calculate the minimum required effective capacitance, C_{OUT}.

$$V_{ripple\_C} = \frac{(V_{OUT} - V_{IN\_MIN}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times C_{OUT}} \quad (9)$$

$$V_{ripple\_ESR} = I_{Lpeak} \times ESR \quad (10)$$

where

- V_{ripple_C} is output voltage ripple caused by charging and discharging of the output capacitor.
- V_{ripple_ESR} is output voltage ripple caused by ESR of the output capacitor.
- V_{IN_MIN} is the minimum input voltage of boost converter.
- V_{OUT} is the output voltage.
- I_{OUT} is the output current.
- I_{Lpeak} is the peak current of the inductor.
- f_{SW} is the converter switching frequency.
- ESR is the ESR resistance of the output capacitors.

Loop Stability

An external loop compensation network comprises resister R5, ceramic capacitors C5 and C6 connected to the COMP pin to optimize the loop response of the converter. The power stage small signal loop response of constant off time with peak current control can be modeled by equation 11.

$$G_{PS}(S) = \frac{R_{load} \times (1-D)}{2 \times R_{SENSE}} \times \frac{(1+\frac{S}{2\pi \times f_{ESRZ}})(1+\frac{S}{2\pi \times f_{RHPZ}})}{1+\frac{S}{2\pi \times f_P}} \quad (11)$$

where

- D is the switching duty cycle.
- R_{load} is the output load resistance.
- R_{SENSE} is the equivalent internal current sense resistor, which is 0.14 Ω.

$$f_P = \frac{1}{2\pi \times R_{load} \times C_O} \quad (12)$$

where

- C_O is the output capacitance

$$f_{PESRZ} = \frac{1}{2\pi \times ESR \times C_O} \quad (13)$$

where

- ESR is the equivalent series resistance of the output capacitor.

$$f_{RHPZ} = \frac{R_{load} \times (1-D)^2}{2\pi \times L} \quad (14)$$

The COMP pin is the output of the internal trans-conductance amplifier. Equation 15 shows the small signal transfer function of compensation network.

$$G_C(S) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{(1+\frac{S}{2\pi \times f_{COMZ}})}{(1+\frac{S}{2\pi \times f_{COMP1}})(1+\frac{S}{2\pi \times f_{COMP2}})} \quad (15)$$

where

- G_{EA} is the amplifier's trans-conductance
- R_{EA} is the amplifier's output resistance
- V_{REF} is the reference voltage at the FB pin
- V_{OUT} is the output voltage
- f_{COMP1}, f_{COMP2} are the poles' frequency of the compensation network.
- f_{COMZ} is the zero's frequency of the compensation network.

The next step is to choose the loop crossover frequency, f_C . The higher frequency that the loop gain stays above zero before crossing over, the faster the loop response is. It is generally accepted that the loop gain cross over no higher than the lower of either 1/10 of the switching frequency, f_{SW} , or 1/5 of the RHPZ frequency, f_{RHPZ}.

Then set the value of R5, C8, and C9 in typical application circuit by following these equations.

$$R_5 = \frac{2\pi \times V_{OUT} \times R_{SENSE} \times f_C \times C_O}{(1-D) \times V_{REF} \times G_{EA}} \quad (16)$$

where

- f_C is the selected crossover frequency.

$$C_5 = \frac{R_{load} \times C_O}{2 \times R_5} \quad (17)$$

$$C_6 = \frac{ESR \times C_O}{R_5} \quad (18)$$

If the calculated value of C6 is less than 10pF, it can be left open. Designing the loop for greater than 45°of phase margin and greater than 10-dB gain margin eliminates output voltage ringing during the line and load transient.

Application Waveforms

Vin=3.6V, Vout=9V, unless otherwise noted

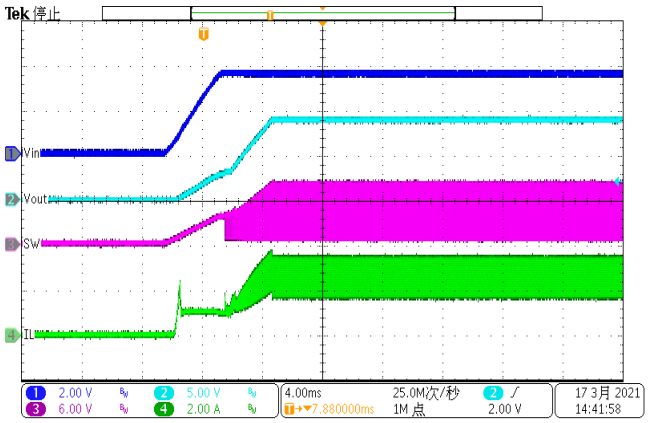


Figure 9. Power up

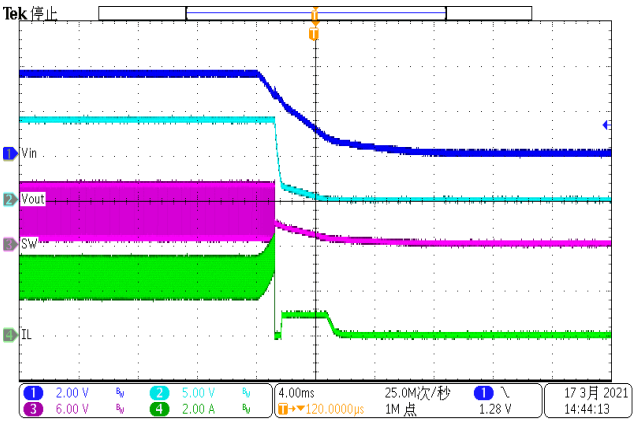


Figure 10. Power down

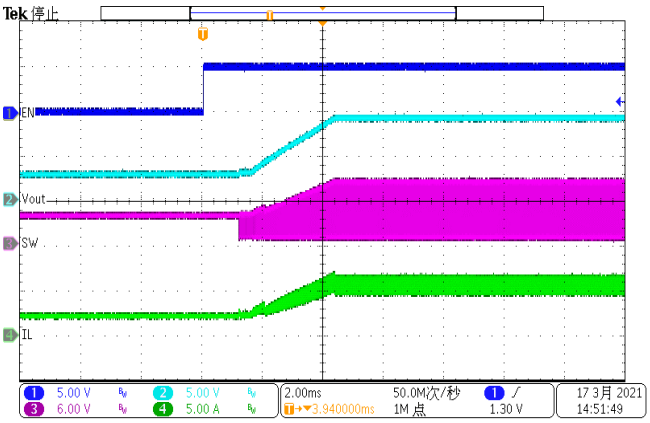


Figure 11. EN Power up (Iload=2A)

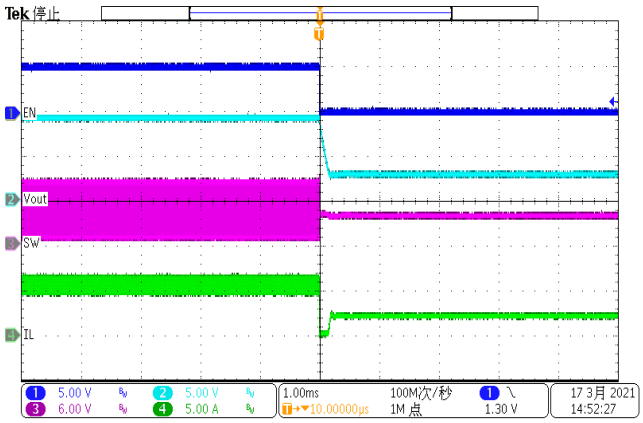


Figure 12. EN Power down(2A)

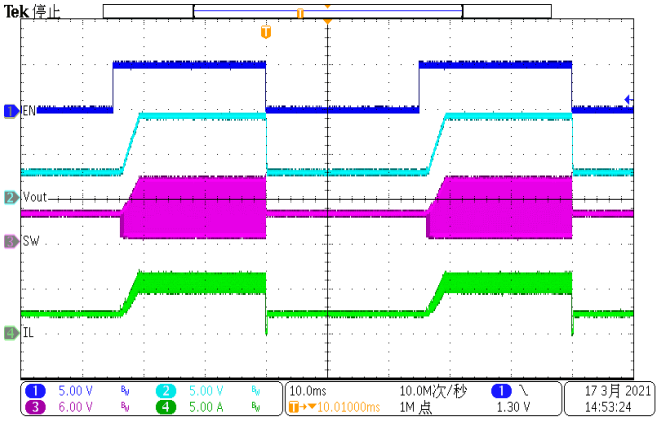


Figure 13. EN toggle (Iload=2A)

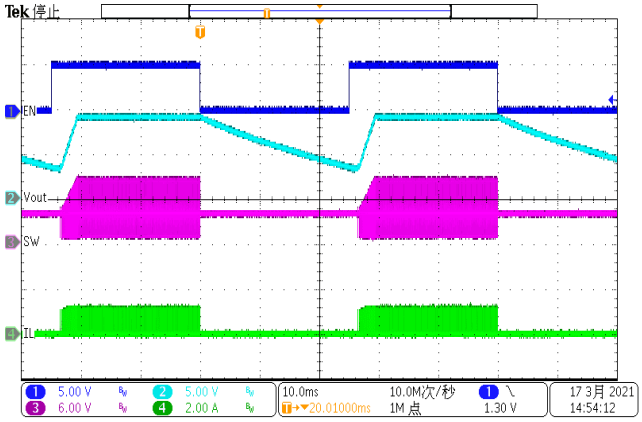


Figure 14. EN toggle (Iload=10mA)

Application Waveforms(continued)

Vin=3.6V, Vout=9V, unless otherwise noted

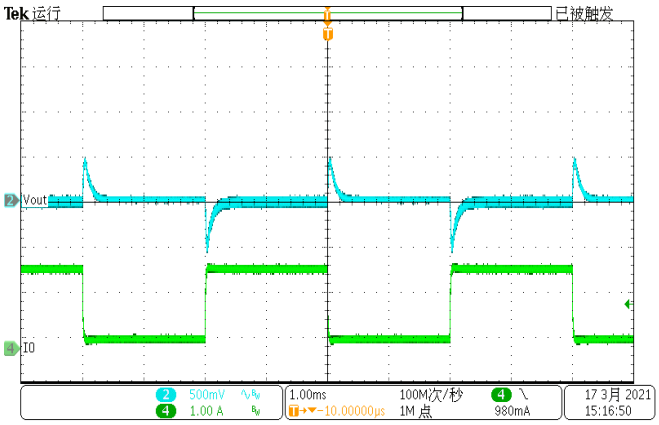


Figure 15. Load transient (0.2A-1.8A, 1.6A/us)

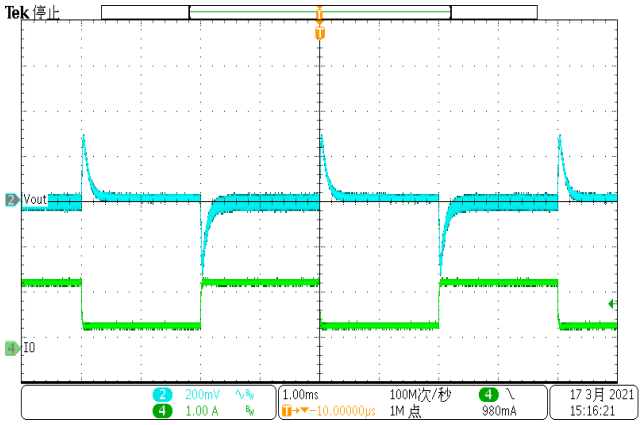


Figure 16. Load transient (0.5A-1.25A, 1.6A/us)

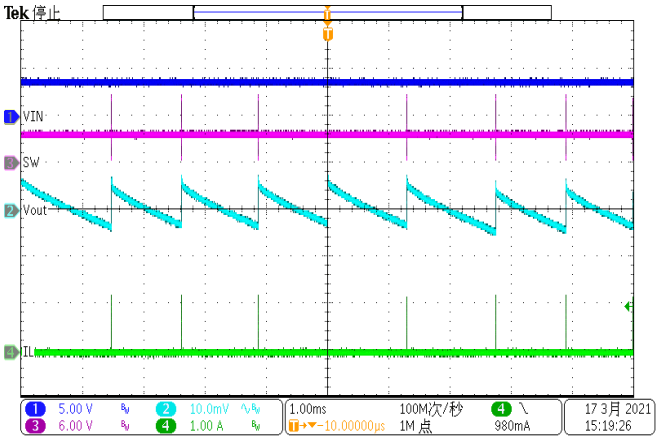


Figure 17. Steady state (Iload=0A, PFM)

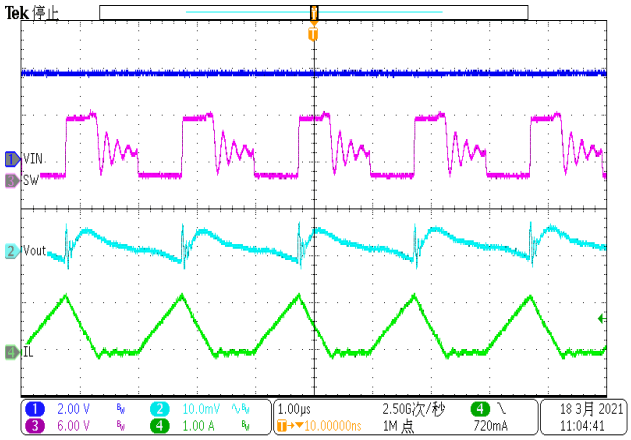


Figure 18. Steady state (Iload=150mA, PFM)

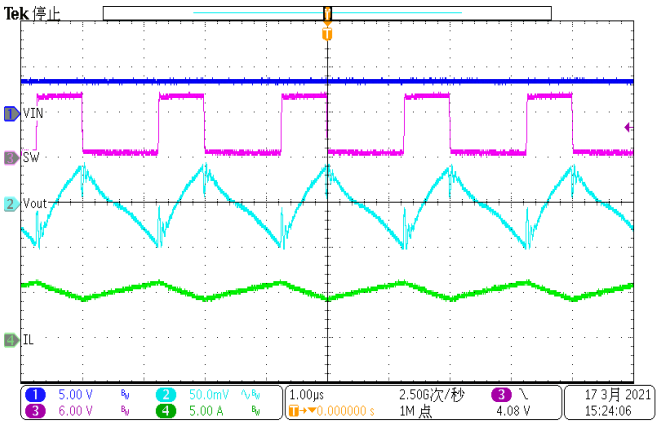


Figure 19. Steady state (Iload=2A)

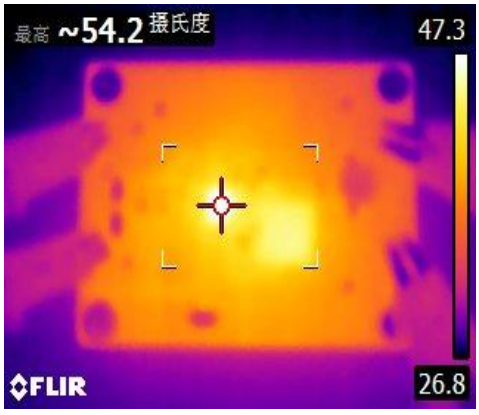


Figure 20. Thermal, Vin=3.6V, Vout=9V, Iload=2A

Layout Guideline

The regulator could suffer from instability and noise problems without careful layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be close to the VIN pin and ground pad to reduce the input supply ripple.

The most critical current path for all boost converters is from the switching FET, through the rectifier FET, then the output capacitors, and back to ground of the switching FET. This high current path contains nanosecond rise time and fall time, and should be kept as short as possible. Therefore, the output capacitor needs not only to be close to the VOUT pin, but also to the GND pin to reduce the overshoot at the SW pin and VOUT pin. The placement and ground trace for output capacitor is critical for the performance of SW ringing voltage. Place the 0.1uF output capacitor as close to VOUT pins and power ground pad as possible to reduce high frequency ringing voltage on SW pin.

The layout should also be done with well consideration of the thermal. The SW, VOUT and GND pad under the chip should always be soldered well to the board for thermal, mechanical strength and reliability. Improper soldering will cause SW higher ringing and overshoot besides downgrading thermal performance.

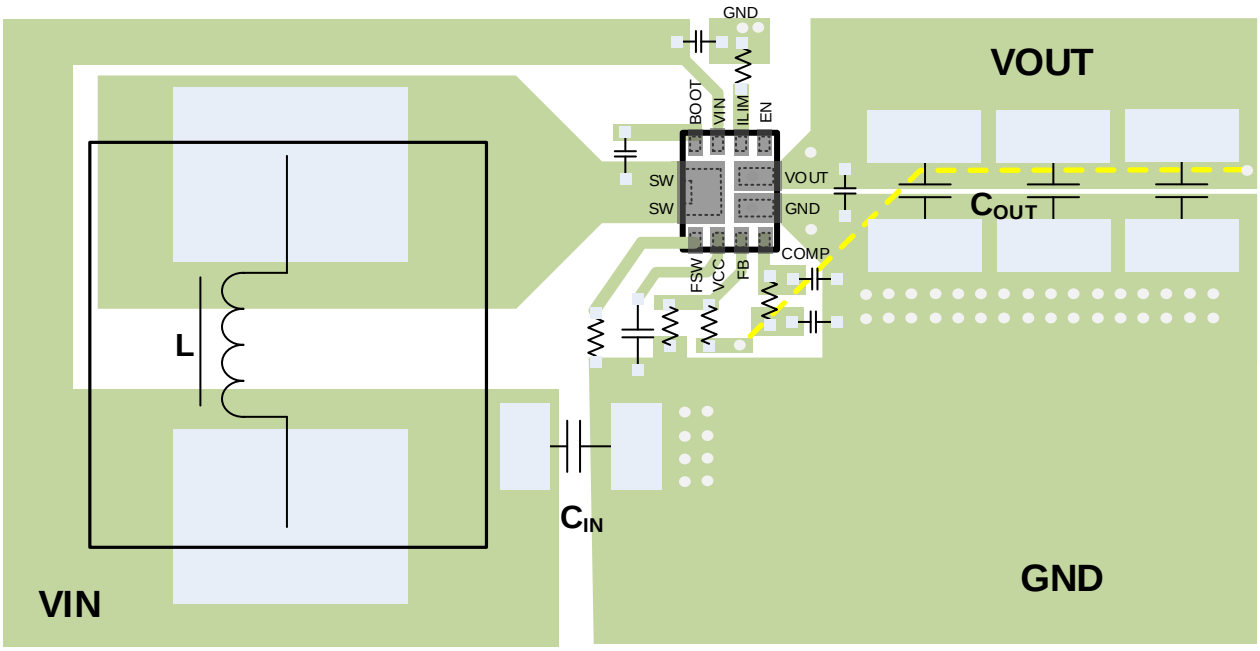


Figure 21. PCB Layout Example Top Layer

Thermal Considerations

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 19.

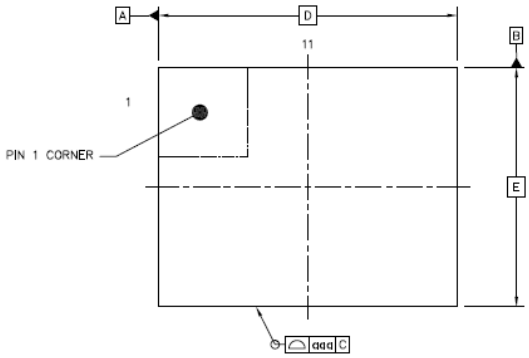
$$P_{D(MAX)} = \frac{150 - TC_A}{R_{\theta JA}} \quad (19)$$

where

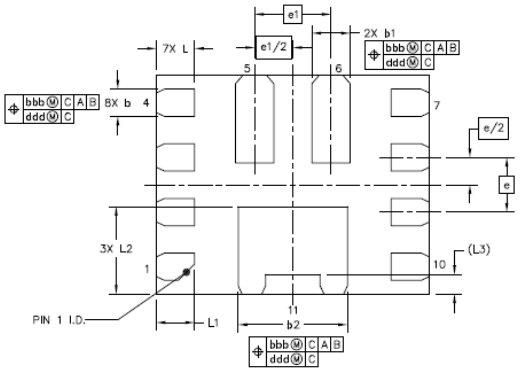
- T_A is the maximum ambient temperature for the application.
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the Thermal Information table.

SCT1271 QFN package includes a thermal pad that improves the thermal capabilities of the package. The real junction-to-ambient thermal resistance $R_{\theta JA}$ of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the thermal pad to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

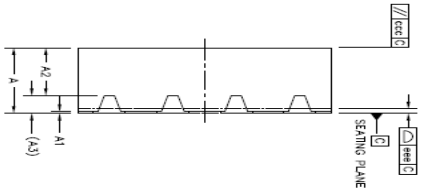
PACKAGE INFORMATION



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	---	0.55	---
A3		0.203 REF	
b	0.20	0.25	0.30
b1	0.30	0.35	0.40
b2	0.95	1	1.05
D		2.5 BSC	
E		2 BSC	
e		0.5 BSC	
e1		0.7 BSC	
L	0.3	0.35	0.4
L1	0.25	0.35	0.45
L2	0.75	0.8	0.85
L3		0.18 REF	
aaa		0.1	
ccc		0.1	
eee		0.05	
bbb		0.1	
ddd		0.05	

TAPE AND REEL INFORMATION