3.8V-36V Vin, 3A Synchronous Step-down DCDC Converter with EMI Reduction

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- 3.8V-36V Wide Input Voltage Range
- Up to 3A Continuous Output Load Current
- EMI Reduction
  - Proprietary Gate Design for Switching Node Ringing-free
  - Frequency Spread Spectrum (FSS)
- Pulse Skipping Mode (PSM) with 22uA Quiescent Current in Light Load Condition
  - Up to 79% Efficiency at 1mA Light Load
  - Up to 89% Efficiency at 10mA Light Load
- 0.8V ±1.5% Feedback Reference Voltage
- Fully Integrated 74mΩ R_{dson} High Side MOSFET and 40mΩ R_{dson} Low Side MOSFET
- 1uA Shut-down Current
- 400kHz Switching Frequency
- Precision Enable Threshold for Programmable UVLO Threshold and Hysteresis
- Output Over Voltage Protection
- Thermal Shutdown Protection at 170°C

APPLICATIONS

- Automotive System
- Industrial Control System

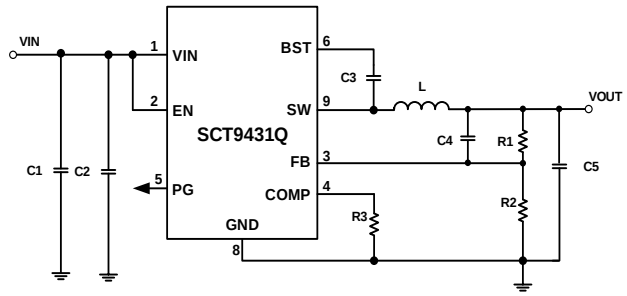
DESCRIPTION

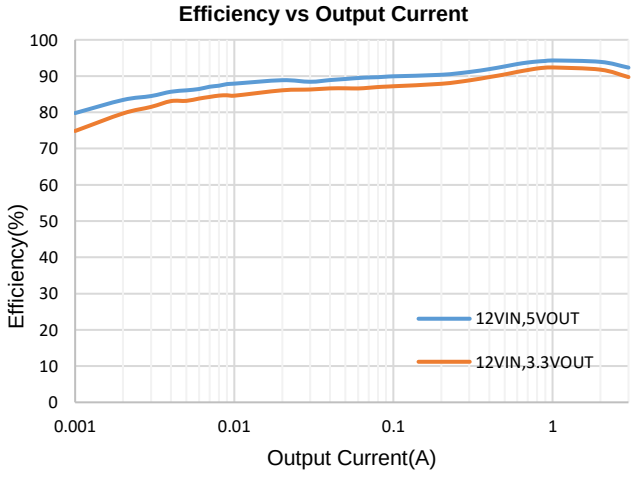
The SCT9431Q are 3A synchronous buck converters with up to 36V wide input voltage range, which fully integrates an 74mΩ high-side MOSFET and a 40mΩ low-side MOSFET to provide high efficiency step-down DCDC conversion. The SCT9431Q adopts peak current mode control with integrated compensation network. The SCT9431Q supports the Pulse Skipping Modulation (PSM) with typical 22uA Ultra-Low Quiescent.

The SCT9431Q are optimized for Electromagnetic Interference (EMI) reduction. The converter has proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching. The converter features Frequency Spread Spectrum (FSS) with a switching frequency jitter of ±6%, which reduces EMI by not allowing emitted energy to stay in any one frequency for a significant period of time.

The SCT9431Q offer output over-voltage protection, cycle-by-cycle peak current limit, and thermal shutdown protection. The device is available in a low-profile QFN-9L 3mm X 2mm package with wettable flanks.

TYPICAL APPLICATION





REVISION HISTORY

Revision 1.0: Production.

Revision 1.1: Update Shutdown current in EC table.

Revision 1.2: Update DEVICE ORDER INFORMATION.

DEVICE ORDER INFORMATION

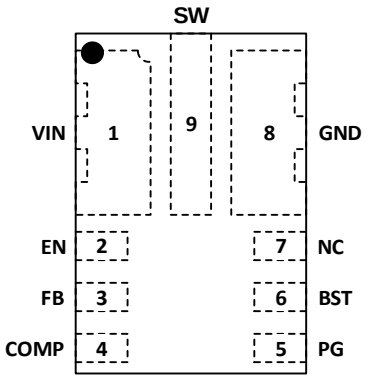
ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT9431QFSAR	Tape & Reel	5000	9431Q	9	FCQFN2x3-9

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
BST	-0.3	48	V
VIN, SW, EN	-0.3	42	V
FB, COMP	-0.3	6	V
BST-SW	-0.3	6	V
Operating junction temperature(2)	-40	125	°C
Junction temperature	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION



Top View: FCQFN2X3-9L

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 170°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
VIN	1	Power supply input. Must be locally bypassed.
EN	2	Enable logic input. Floating the pin enables the device. This pin supports high voltage input up to VIN supply to be connected VIN directly to enable the device automatically. The device has precision enable thresholds 1.18V rising / 1.1V falling for programmable UVLO threshold and hysteresis.
FB	3	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference of 0.8V typical.
COMP	4	Compensation pin. Connect this pin to GND with a 1KΩ resistor for internal compensation. Add an RC network to adjust the loop response externally. See Loop Response Design for more details.
PG	5	Open drain power-good output that is pulled to GND when the output voltage is out of its regulation limits or during soft-start. There is an internal 5MΩ pull-up resistor.

BST	6	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BST pin and SW node.
NC	7	NC
GND	8	Power ground. Must be soldered directly to ground plane.
SW	9	Switching node of the buck converter.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.8	36	V
T_A	Operating Ambient Temperature Range	-40	125	°C
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(1)	-1	+1	kV

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	QFN-9L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	61.33	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.24	
Ψ_{JB}	Junction-to-board characterization parameter(1)	5.43	
$R_{\theta JCtop}$	Junction to case(top) thermal resistance(1)	62.99	
$R_{\theta JB}$	Junction-to-board thermal resistance(1)	5.6	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT9431Q is mounted. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT9431Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C~150°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		3.8		36	V
V_{IN_UVLO}	Input UVLO	V_{IN} rising	3.3	3.5	3.7	V
	Hysteresis			420		mV
I_{SD}	Shutdown current	EN=0, No load, VIN=12V		0.6	5	uA
I_Q	Quiescent current	EN=floating, No load, No switching. VIN=12V. BST-SW=5V		22	40	uA
Enable, Soft Start and Working Modes						
V_{EN_H}	Enable high threshold		1.08	1.18	1.28	V
V_{EN_L}	Enable low threshold		0.98	1.1	1.18	V
I_{EN_L}	Enable pin input current	EN=1V	1	1.5	2	uA
I_{EN_H}	Enable pin input current	EN=1.5V		4		uA
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			74	130	mΩ
R_{DSON_L}	Low side FET on-resistance			40	70	mΩ
Feedback and Error Amplifier						
V_{FB}	Feedback Voltage	T_J =25℃	0.792	0.8	0.808	V
		T_J =-40℃-150℃	0.788	0.8	0.812	V
Current Limit						
I_{LIM_HSD}	HSD peak current limit	T_J =25℃	4.0	4.5	5.0	A
		T_J =-40℃-150℃	3.7	4.5	5.3	A
I_{LIM_LSD}	LSD valley current limit			4		A
Switching Frequency						
F_{SW}	Switching frequency	V_{IN}=12V, V_{OUT}=5V, T_J =25℃	350	400	450	kHz
		V_{IN}=12V, V_{OUT}=5V, T_J =-40℃-150℃	330		470	
t_{ON_MIN}	Minimum on-time			100		ns
Soft Start Time						
t_{SS}	Internal soft-start time			4		ms
Protection						
V_{OVP}	Output OVP threshold	V_{OUT} rising Hysteresis		110 5		% %
T_{SD}	Thermal shutdown threshold*	T_J rising Hysteresis		170 25		°C

*Derived from bench characterization

TYPICAL CHARACTERISTICS

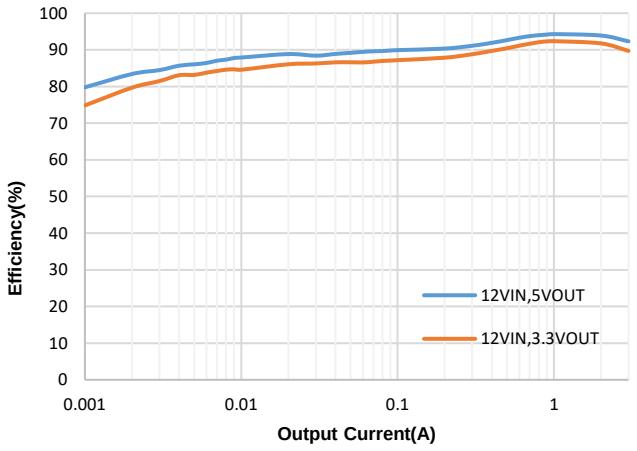


Figure 1. Efficiency vs Load Current

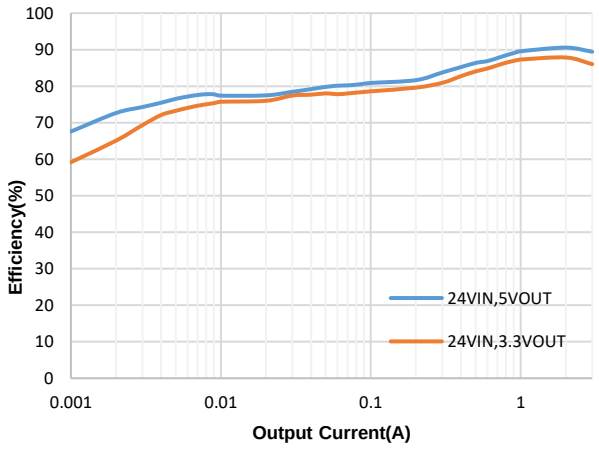


Figure 2. Efficiency vs Load Current

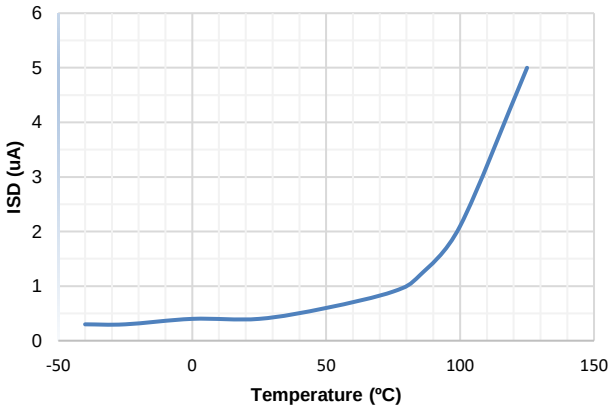


Figure 3. Shut-down Current vs Temperature

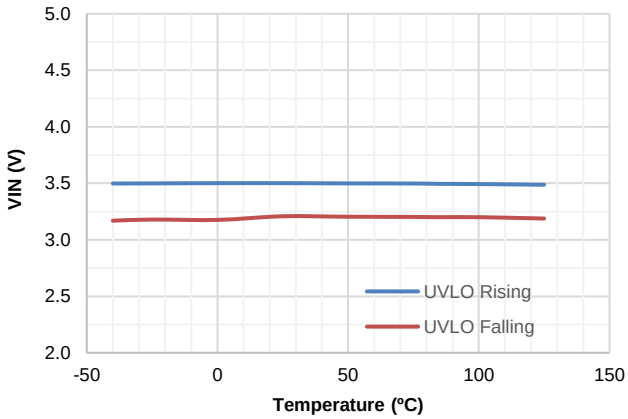


Figure 4. VIN UVLO vs Temperature

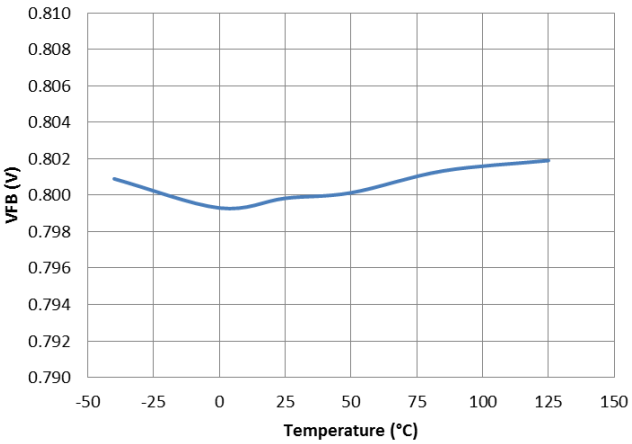


Figure 5. Reference Voltage vs Temperature

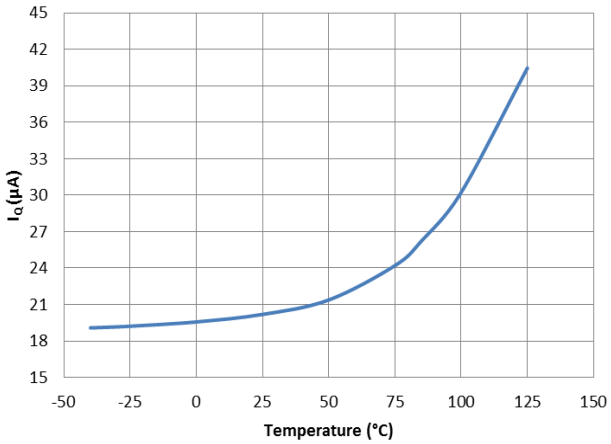


Figure 6. I_Q vs. Temperature, IOUT = 0A

FUNCTIONAL BLOCK DIAGRAM

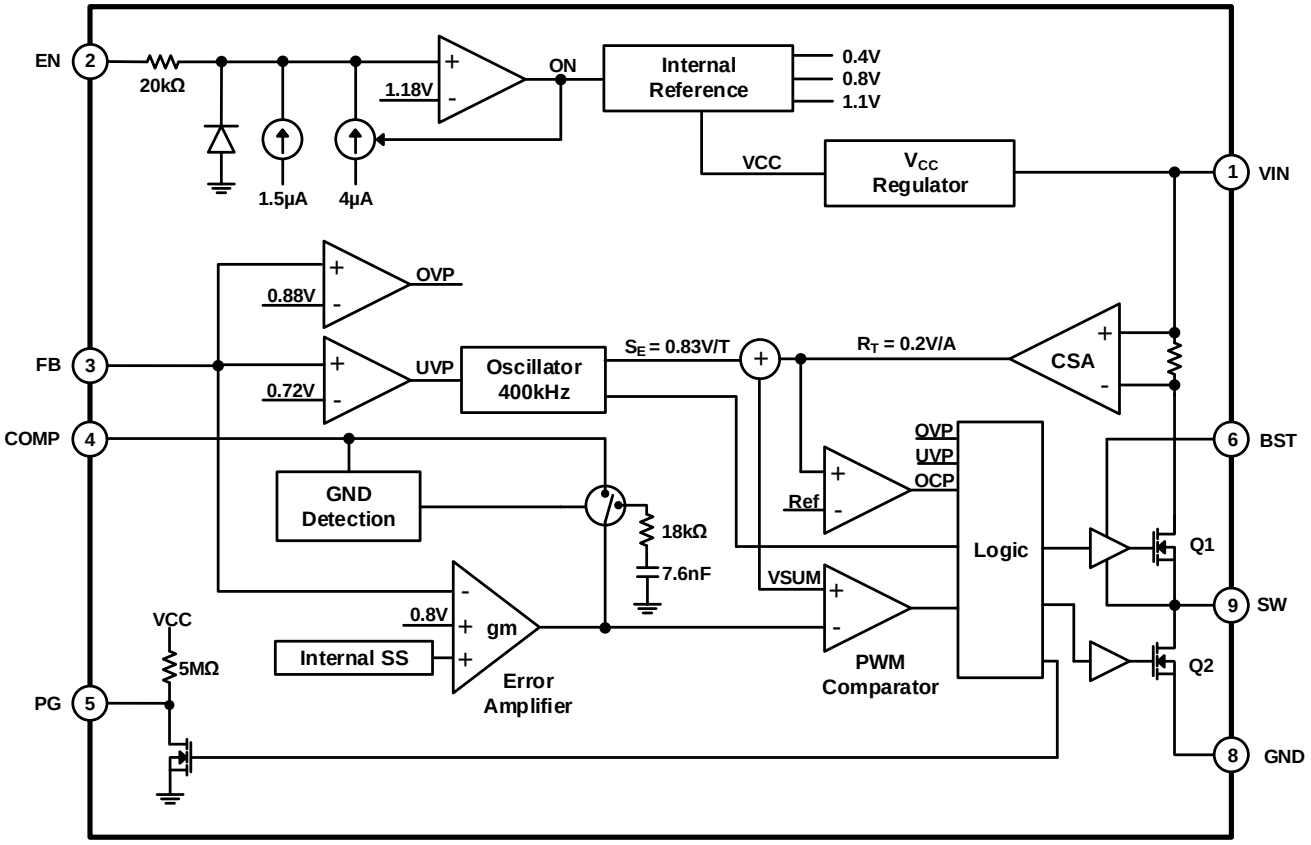


Figure 7. Functional Block Diagram

OPERATION

Overview

The SCT9431Q device is 3.8V-36V input, 3A output, EMI friendly, fully integrated synchronous buck converters. The device employs fixed frequency peak current mode control. An internal clock with 400kHz frequency initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly and the converter charges output cap. When sensed voltage on high-side MOSFET peak current via the CSA block, rising above the voltage of internal COMP (see functional block diagram), the device turns off high-side MOSFET Q1 and turns on low-side MOSFET Q2. The inductor current decreases when MOSFET Q2 is ON. In the next rising edge of clock cycle, the low-side MOSFET Q2 turns off. This repeats on cycle-by-cycle based.

The internal loop compensation network and the built-in 4ms soft-start simplify the SCT9431Q footprints, and minimize the off-chip component counts. The quiescent current of SCT9431Q is 22uA typical under no-load condition and no switching. When disabling the device, the shutdown current of SCT9431Q is only 1μA. The SCT9431Q works at Pulse Skipping Mode PSM to further increase the power efficiency in light load condition, hence the power efficiency can be achieved up to 88% at 5mA load condition.

The error amplifier serves the COMP node by comparing the voltage on the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The SCT9431Q device implements Frequency Spread Spectrum (FSS) with a switching frequency jitter of ±6%. FSS reduces EMI by not allowing emitted energy to stay in any one frequency for a significant period of time. The converter further dampens high frequency radiated EMI noise through the use of its proprietary gate driver scheme to achieve a ringing-free switching node voltage without sacrificing the MOSFET switching times.

The hiccup mode minimizes power dissipation during prolonged output overcurrent or short conditions. The hiccup wait time is 512 cycles and the hiccup restart time is 8192 cycles. The SCT9431Q device also features protections including cycle-by-cycle high-side MOSFET peak current limit, over-voltage protection, and over-temperature protection.

PSM Working Modes

In heavy load condition, the SCT9431Q forces the device operating at PWM mode. When the load current decreasing, the internal COMP net voltage decreases as the inductor current down. With the load current further decreasing, the COMP net voltage decreases and be clamped at a voltage corresponding to the 600mA peak inductor current. When the load current approaches zero, the SCT9431Q enter Pulse Skipping Mode (PSM) mode to increase the converter power efficiency at light load condition. When the inductor current decreases to zero, zero-cross detection circuitry on high-side MOSFET Q1 forces the Q1 off till the beginning of the next switching cycle. The buck converter does not sink current from the load when the output load is light and converter works in PSM mode.

VIN Power

The SCT9431Q is designed to operate from an input voltage supply range between 3.8V to 36V. At least a 0.1uF decoupling ceramic cap is recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional electrolytic or tantalum bulk capacitor or with recommended 22uF may be required in addition to the local ceramic bypass capacitors.

Under Voltage Lockout UVLO

The SCT9431Q Under Voltage Lock Out (UVLO) default startup threshold is typical 3.5V with VIN rising and shutdown threshold is 3.1V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin.

Enable and Start up

When applying a voltage higher than the EN high threshold (typical 1.18V/rise), the SCT9431Q enables all functions and the device starts soft-start phase. The SCT9431Q has the built in 4ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.1V/fall).

An internal 1.5uA pull up current source connected from internal LDO power rail to EN pin guarantees that floating EN pin automatically enables the device. For the application requiring higher VIN UVLO voltage than the default setup, there is a 4uA hysteresis pull up current source on EN pin which configures the VIN UVLO voltage with an off-chip resistor divider R3 and R4, shown in Figure 8. The resistor divider R3 and R4 are calculated by equation (1) and (2).

EN pin is a high voltage pin and can be directly connected to VIN to automatically start up the device with VIN rising to its internal UVLO threshold.

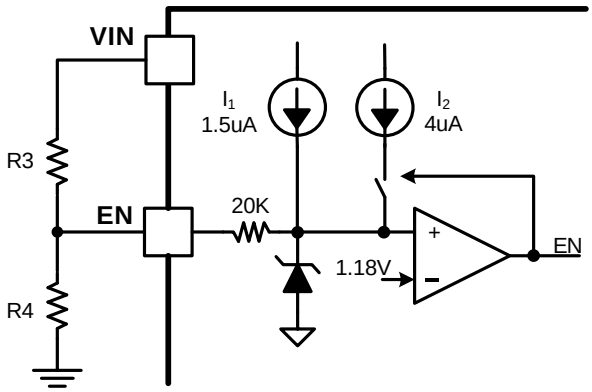


Figure 8. Adjustable VIN UVLO

$$R3 = \frac{V_{Start}\left(\frac{V_{ENF}}{V_{ENR}}\right) - V_{Stop}}{I_1\left(1 - \frac{V_{ENF}}{V_{ENR}}\right) + I_2} \quad (1)$$

$$R4 = \frac{R_3 \times V_{ENF}}{V_{Stop} - V_{ENF} + R_3(I_1 + I_2)} \quad (2)$$

Where:

- V_{start}: Vin rise threshold to enable the device
- V_{stop}: Vin fall threshold to disable the device
- I_1=1.5uA
- I_2=4uA
- V_{ENR}=1.18V
- V_{EMF}=1.1V

Power-GOOD (PG) Indicator

The SCT9431Q has an open-drain output that is actively held low during soft start period until the output voltage reaches 90% of the target output. When the output voltage is outside of its regulation by -10%, the PG will pull low until the output returns to set value. The PG low to high transition is delayed by 2.5ms while the falling edge PG is

delayed by 220μs to prevent false triggering.

Peak Current Limit and Hiccup Mode

The SCT9431Q have cycle-by-cycle peak current limit with sensing the internal high side MOSFET Q1 current during overcurrent condition. While the Q1 turns on, its conduction current is monitored by the internal sensing circuitry. Once the high-side MOSFET Q1 current exceeds the limit, it turns off immediately. If the Q1 over current time exceeds 512 switching cycles (hiccup waiting time), the buck converter enters hiccup mode and shuts down. After 8192 cycles off, the buck converter restarts to power up. The hiccup modes reduce the power dissipation in over current condition.

Over Voltage Protection and Minimum On-time

Both SCT9431Q feature output over voltage protection (OVP). If the output feedback pin voltage exceeds 110% of feedback reference voltage, the converter stops switching immediately. When the output feedback pin voltage drops below 105% of feedback reference voltage, the converter resumes to switching. The OVP function prevents the connected output circuitry damaged from un-predictive overvoltage. Featured feedback overvoltage protection also prevents dynamic voltage spike to damage the circuitry at load during fast loading transient.

The high-side MOSFET Q1 has minimum on-time 100ns typical limitation. While the device operates at minimum on-time, further increasing VIN results in pushing output voltage beyond regulation point. With output feedback over voltage protection, the converter skips pulse by turning off high-side MOSFET Q1 and prevents output running away higher to damage the load.

Bootstrap Voltage Regulator

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The floating supply (BST to SW) UVLO threshold is 2.7V rising and hysteresis of 350mV. When the converter operates with high duty cycle or prolongs in sleep mode for certain long time, the required time interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 2.35V, BST UVLO occurs. The SCT9431Q intervenes to turn on low side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee operation over a wide duty range.

EMI Reduction with Switching Node Ringing-free

In buck converter, the switching node ringing amplitude and cycles are critical especially related to the high frequency radiation EMI noise. The SCT9431Q implements the multi-level gate driver speed technique to achieve the switching node ringing-free without scarifying the switching node rise/fall slew rate and power efficiency of the converter. The switching node ringing amplitude and cycles are damped by the built-in MOSFETs gate driving technique (SCT Patented Proprietary Design).

Thermal Shutdown

Once the junction temperature in the SCT9431Q exceeds 170°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 145°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

APPLICATION INFORMATION

Typical Application

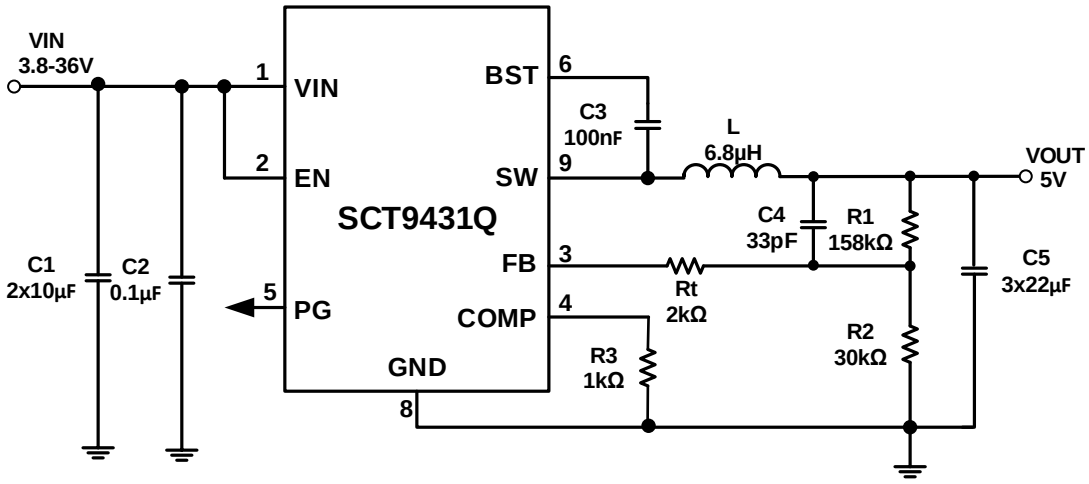


Figure 9. 12V Input, 5V/3A Output with Internal Compensation

Design Parameters

Design Parameters	Example Value
Input Voltage	12V
Output Voltage	5V
Output Current	3A
Output voltage ripple (peak to peak)	±0.03V
Switching Frequency	400kHz

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10μF is recommended for the decoupling capacitor and a 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT9431Q.

Use Equation (3) to calculate the input voltage ripple:

$$\Delta V_{IN} = \frac{I_{OUT}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where:

- C_{IN} is the input capacitor value
- f_{sw} is the converter switching frequency
- I_{OUT} is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to make sure the input voltage ripple less than 100mV. Generally, a 35V/10uF input ceramic capacitor is recommended for most of applications. Choose the right capacitor value carefully with considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Inductor Selection

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and buck converter efficiency. The inductor value, DC resistance (DCR), and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DCR, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the maximum input voltage, minimum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a buck converter, calculate the inductor minimum value as shown in equation (4).

$$L_{INDMIN} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times K_{IND} \times I_{OUT} \times f_{SW}} \quad (4)$$

Where:

- K_{IND} is the coefficient of inductor ripple current relative to the maximum output current.

Therefore, the peak switching current of inductor, I_{LPEAK}, is calculated as in equation (5).

$$I_{LPEAK} = I_{OUT} + K_{IND} \times \frac{I_{OUT}}{2} \quad (5)$$

Set the current limit of the SCT9431Q higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit. The inductor's DC resistance (DCR) and the core loss significantly affect the efficiency of power conversion. Core loss is related to the core material and different inductors have different core

loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss.

Output Capacitor Selection

For buck converter, the output capacitor value determines the regulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor, for example, X5R and X7R family. Typically, 1～2x 22μF ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. Due to a capacitor's de-rating under DC bias, the bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance.

From the required output voltage ripple, use the equation (6) to calculate the minimum required effective capacitance, C_{OUT}.

$$C_{OUT} = \frac{\Delta I_{LPP}}{8 \times V_{OUTRipple} \times f_{SW}} \quad (6)$$

Where

- $V_{OUTRipple}$ is output voltage ripple caused by charging and discharging of the output capacitor.
- ΔI_{LPP} is the inductor peak to peak ripple current, equal to k_{IND} * I_{OUT}.
- f_{SW} is the converter switching frequency.

The allowed maximum ESR of the output capacitor is calculated by the equation (7).

$$R_{ESR} = \frac{V_{OUTRipple}}{\Delta I_{LPP}} \quad (7)$$

The output capacitor affects the crossover frequency f_C. Considering the loop stability and effect of the internal loop compensation parameters, choose the crossover frequency less than 40 kHz ($\frac{1}{10} \times f_{SW}$) without considering the feed-forward capacitor. A simple estimation for the crossover frequency without feed forward capacitor is shown in equation (8), assuming C_{OUT} has small ESR.

$$C_{OUT} > \frac{18k \times G_M \times G_{MP} \times 0.8V}{2\pi \times V_{OUT} \times f_C} \quad (8)$$

Where

- G_M is the transfer conductance of the error amplifier (300uS).
- G_{MP} is the gain from internal COMP to inductor current, which is 5A/V.
- f_C is the cross over frequency.

Additional capacitance de-rating for aging, temperature and DC bias should be factored in which increases this minimum value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. The capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. Equation (9) can be used to calculate the RMS ripple current the output capacitor needs to support.

$$I_{COUTRMS} = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{\sqrt{12} \cdot V_{IN} \cdot L_{IND} \cdot f_{SW}} \quad (9)$$

Output Feed-Forward Capacitor Selection

The SCT9431Q has the internal integrated loop compensation as shown in the function block diagram. The compensation network includes a 18k resistor and a 7.6nF capacitor. Usually, the type II compensation network has a phase margin between 60 and 90 degree. However, if the output capacitor has ultra-low ESR, the converter results in low phase margin. To increase the converter phase margin, a feed-forward cap C_{ff} is used to boost the phase margin at the converter cross-over frequency f_c. Equation (10) is used to calculate the feed-forward capacitor.

$$C_{ff} = \frac{1}{2\pi \cdot f_C \times R_1} \quad (10)$$

Output Feedback Resistor Divider Selection

The SCT9431Q features external programmable output voltage by using a resistor divider network R1 and R2 as shown in the typical application circuit Figure 9. Use equation (11) to calculate the resistor divider values.

$$R_1 = \frac{(V_{OUT} - V_{ref}) \times R_2}{V_{ref}} \quad (11)$$

Set the resistor R2 value to be approximately 30k. Slightly increasing or decreasing R1 can result in closer output voltage matching when using standard value resistors.
Table 1 is the recommend external components for the application with integrated loop compensation for SCT9431Q.

Table 1. Recommended External Components with Internal Compensation

Vout	L1	COUT	R1	R2	Rt	R3	C4
1.2V	2.2uH	3*22uF	15k	30k	2k	1k	/
3.3V	5.6uH	3*22uF	95k	30k	2k	1k	47pF
5V	6.8uH	3*22uF	158k	30k	2k	1k	33pF
12V	15uH	4*22uF	422k	30k	2k	1k	/

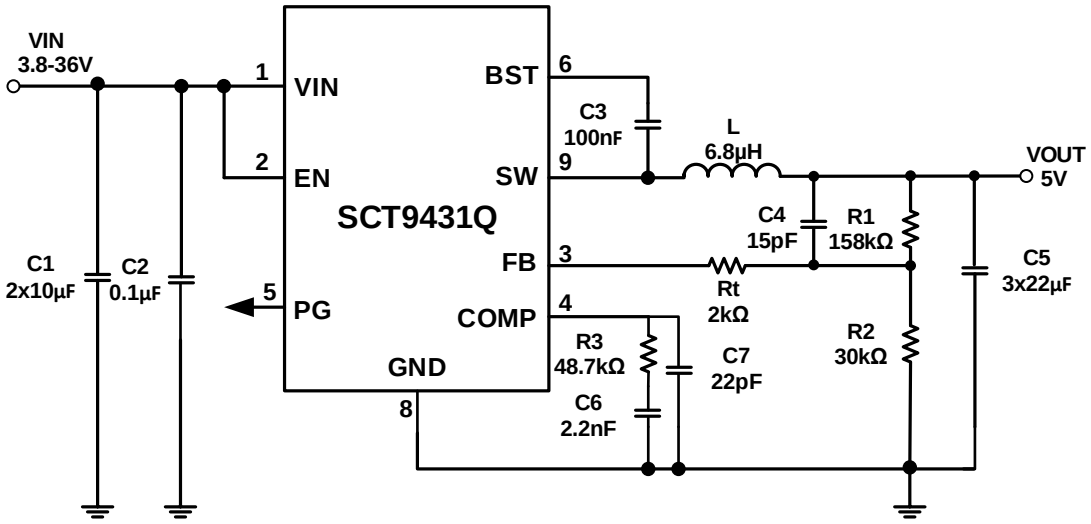


Figure 10. 12V Input, 5V/3A Output with External Compensation

Loop Response Design

When the COMP pin is not connected to GND, the COMP pin is active for external loop compensation. The regulator uses constant frequency peak current mode control architecture to achieve a fast loop response. The inductor is not considered as a state variable since its peak current is constant. The system becomes a single order system. It is much easier to design a type II compensator (Figure 12) to stabilize the loop than in case of a voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 11 shows the small signal model of the synchronous buck regulator.

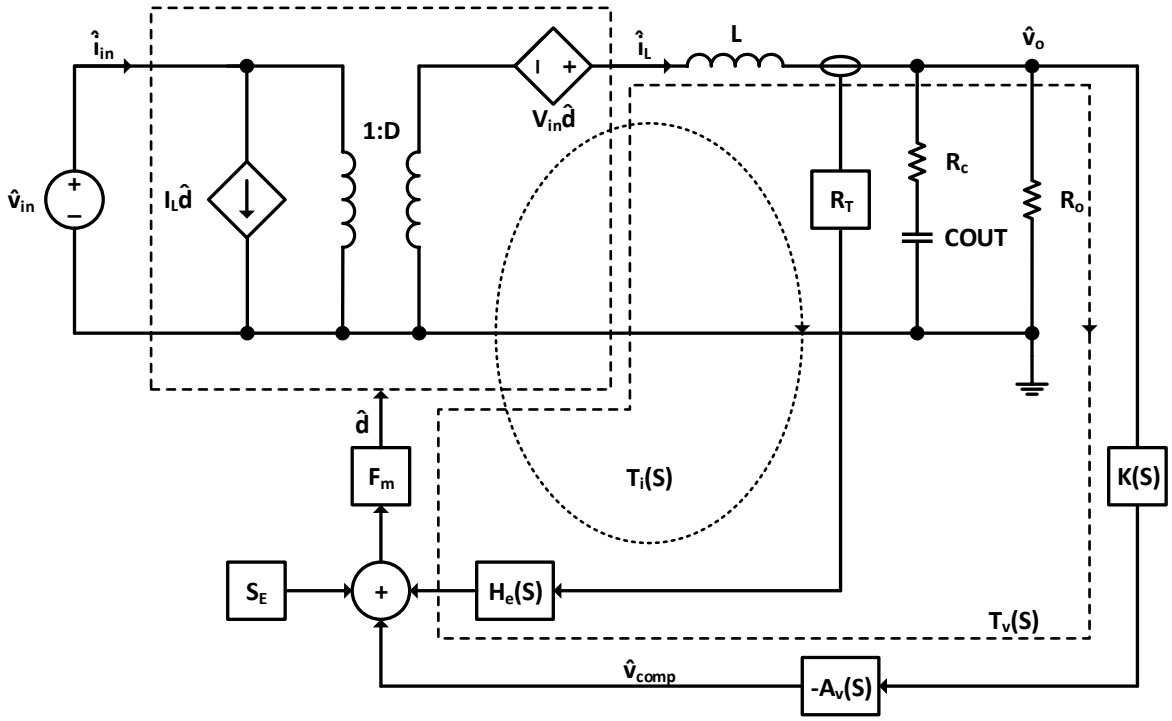


Figure 11. Small Signal Model of Buck Regulator

Where:

- $T_v(S)$ is the voltage loop
- $T_i(S)$ is the current loop
- $K(S)$ is the voltage sense gain
- $-A_v(S)$ is the feedback compensation gain
- $H_e(S)$ is the current sampling function
- F_m is the PWM comparator gain
- V_{in} is the DC input voltage
- D is the duty cycle
- R_c is the ESR of the output capacitor, COUT
- R_o is the output load resistance$\hat{v}_{in}$ is the AC small-signal input voltage
- $\hat{i}_{in}$ is the AC small-signal input current
- $\hat{d}$ is the modulation of the duty cycle
- $\hat{i}_L$ is the AC small signal of the inductor current
- $\hat{v}_o$ is the AC small signal of output voltage
- $\hat{v}_{comp}$ is the AC small signal voltage of the compensation network

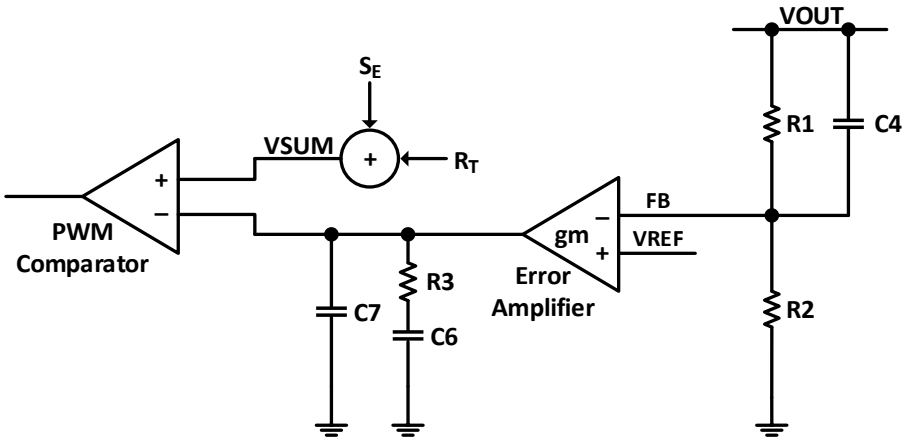


Figure 12. Type II Compensator

Transfer function of Figure 12 is expressed in the following equation,

$$A(S) = \frac{\hat{V}_{COMP}}{\hat{V}_{FB}} = \frac{gm \cdot R3}{(C6 + C7) \cdot (R1 + R2)} \frac{\left(1 + \frac{S}{\omega_{z1}}\right)\left(1 + \frac{S}{\omega_{z2}}\right)}{S \cdot \left(1 + \frac{S}{\omega_{p1}}\right)\left(1 + \frac{S}{\omega_{p2}}\right)} \quad (12)$$

Where:

$$\omega_{z1} = \frac{1}{R3 \cdot C6}$$

$$\omega_{z2} = \frac{1}{R1 \cdot C4}$$

$$\omega_{p1} = \frac{C6 + C7}{R3 \cdot C6 \cdot C7}$$

$$\omega_{p2} = \frac{R1 + R2}{R1 \cdot R2 \cdot C4}$$

The goal of loop compensation design is to achieve:

- High DC Gain
- Gain Margin less than -10dB
- Phase Margin greater than 45°
- Loop Bandwidth Crossover Frequency (f_c) less than 40kHz (10% of f_{sw})

The loop gain at crossover frequency of fc has a unity gain. Therefore, the compensator resistance R3 is determined by equation below. A recommended rule of thumb is to set the crossover frequency to be approximately 1/5 to 1/10 of switching frequency.

$$R3 = \frac{2\pi \cdot fc \cdot Vout \cdot Co \cdot Rt}{gm \cdot VFB} \quad (13)$$

Where

- gm=0.3mS,
- Rt=0.2V/A
- VFB=0.8V,
- fc is the desired crossover frequency
- Vout is the output voltage
- Co is the effective output capacitance.

Be cautioned that most ceramic will degrade with voltage stress or temperature extremes.

The compensator capacitor C6 and C7 are then equal to:

$$C6 = \frac{Vout \cdot Co}{Io \cdot R3}, \quad C7 = max\left[\frac{Rc \cdot Co}{R3}, \frac{1}{\pi \cdot fsw \cdot R3}\right] \quad (14)$$

Where :

- Io is the output load current
- Rc is the ESR equivalent of the Co
- Fs is the switching frequency. In most cases, C7 can omit.

An optional zero, ωz2, can boost the phase margin but it can also increase the gain crossover. Place this zero at 2 to 5 times the fc. Then C4 is equal to:

$$C4 = \frac{1}{10\pi \cdot fc \cdot R1} \ to \ \frac{1}{4\pi \cdot fc \cdot R1} \quad (15)$$

Table 2. Recommended External Components with External Compensation

Vout	L1	COUT	R1	R2	Rt	C4	R3	C6	C7
1.2V	2.2uH	3*22uF	15k	30k	2k	/	20k	1.5nF	/
3.3V	5.6uH	3*22uF	95k	30k	2k	33pF	31.6k	2.2nF	33pF
5V	6.8uH	3*22uF	158k	30k	2k	15pF	48.7k	2.2nF	22pF
12V	15uH	4*22uF	422k	30k	2k	10pF	97.6k	3.3nF	22pF

Application Waveforms

Vin=12V, Vout=5V, unless otherwise noted

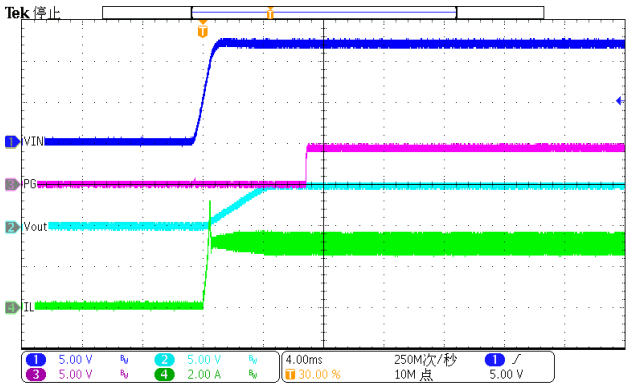


Figure 13. Power up(Iload=3A)

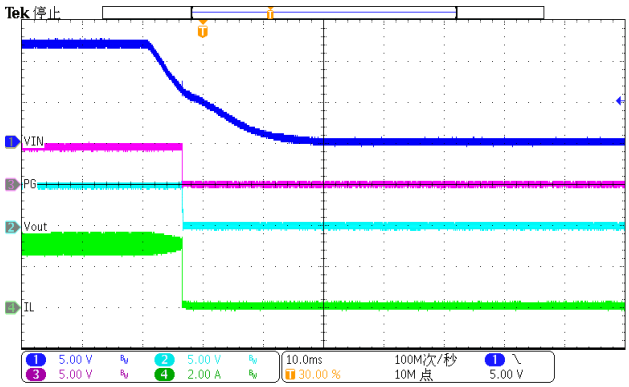


Figure 14. Power down(Iload=3A)

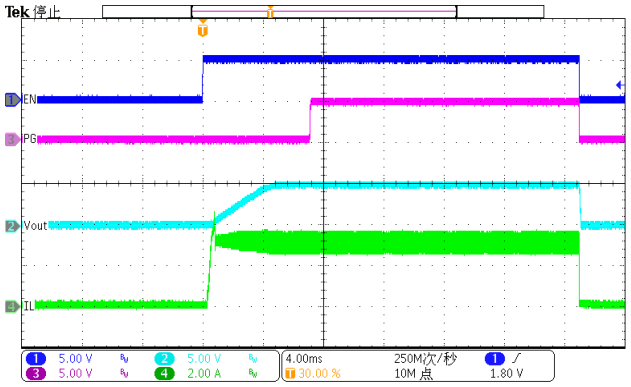


Figure 15.Enable (Iload=3A)

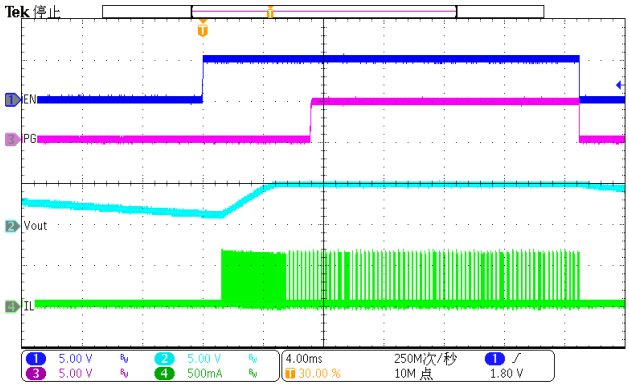


Figure 16. Enable (Iload=10mA)

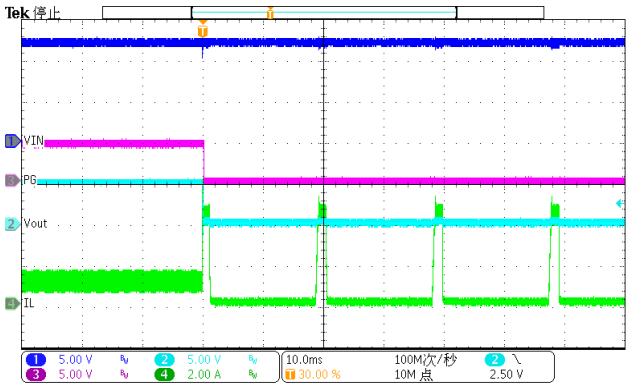


Figure17. Normal to Hard Short

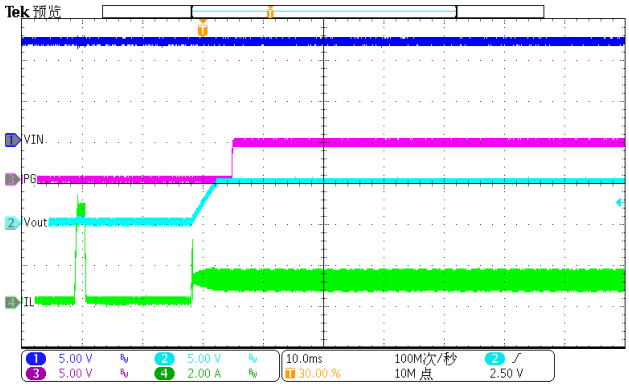


Figure 18. Hard Short Recovery

Application Waveforms(continued)

Vin=12V, Vout=5V, unless otherwise noted

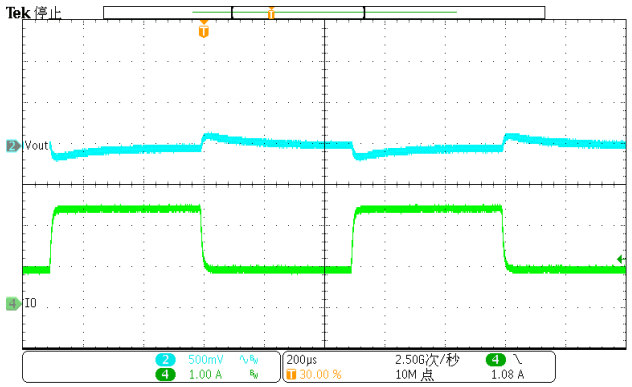


Figure 19. Load Transient (0.75A-2.25A, 1.6A/us)

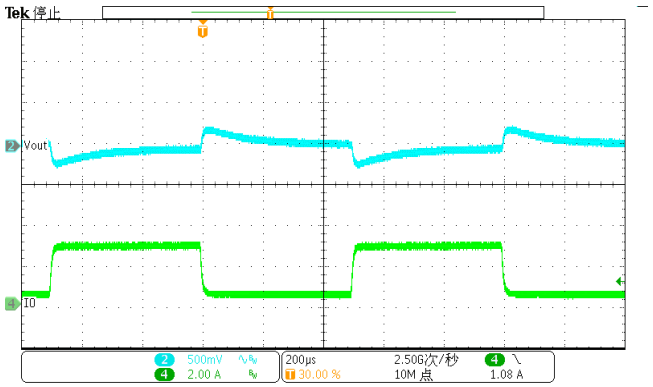


Figure 20. Load Transient (0.3A-2.7A, 1.6A/us)

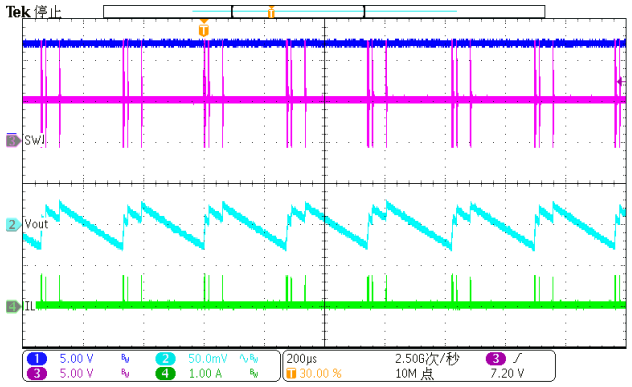


Figure 21. Output Ripple (Iload=10mA)

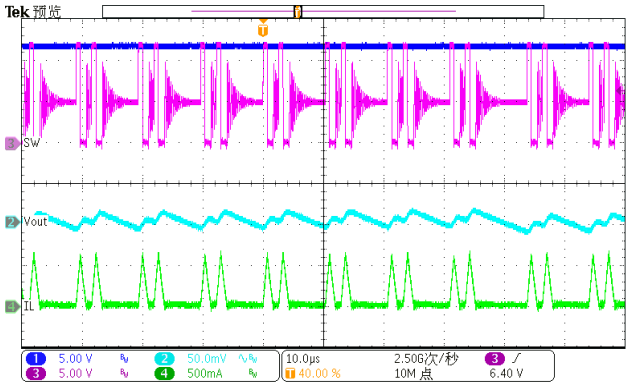


Figure 22. Output Ripple (Iload=0.1A)

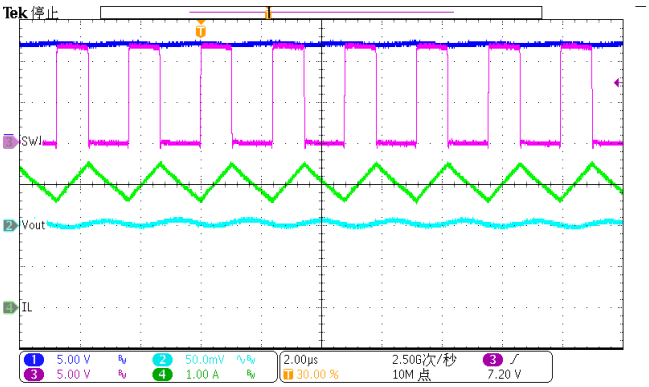


Figure 23. Output Ripple (Iload=3A)

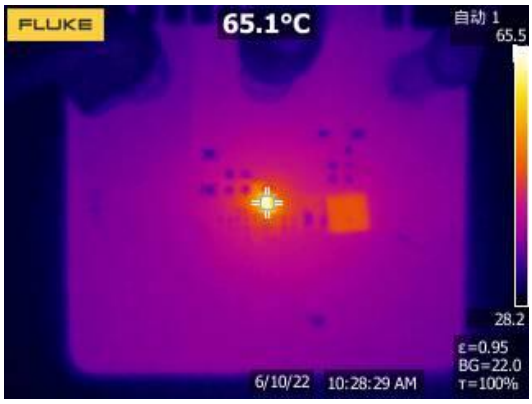


Figure 24. Thermal, 12VIN, 5Vout, 3A

Layout Guideline

Figure 25 and Figure 26 are the recommended PCB layout of SCT9431Q with or without external compensation network.

1. The SCT9431Q works at 3A load current so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Place the input capacitors as closely across VIN and GND as possible.
3. Place the inductor as close to SW as possible.
4. Place the output capacitors as close to GND as possible.
5. Place the feedback components as close to FB as possible.
6. If using four or more layers, use at least the 2nd and 3rd layers as GND to maximize thermal performance.
7. Add as many vias under both the thermally exposed GND pad and GND plane for heat dissipation to all the GND layers.
8. Add as many vias under both the thermally exposed VIN pad and VIN plane for heat dissipation to all the VIN layers.

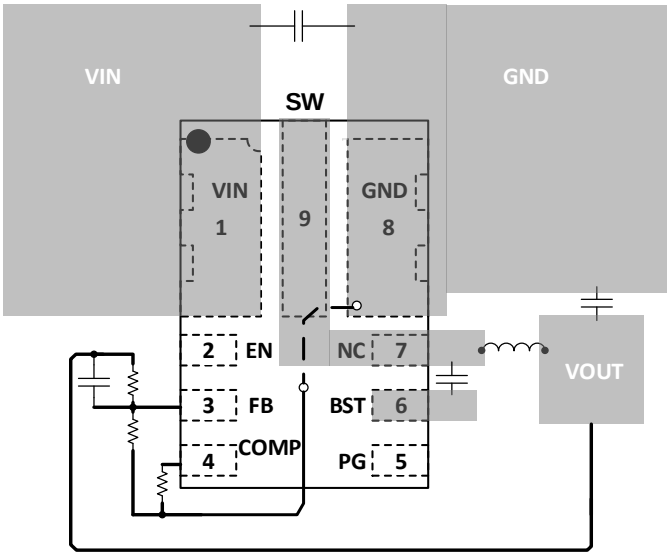


Figure 25. PCB Layout Example for application with internal compensation

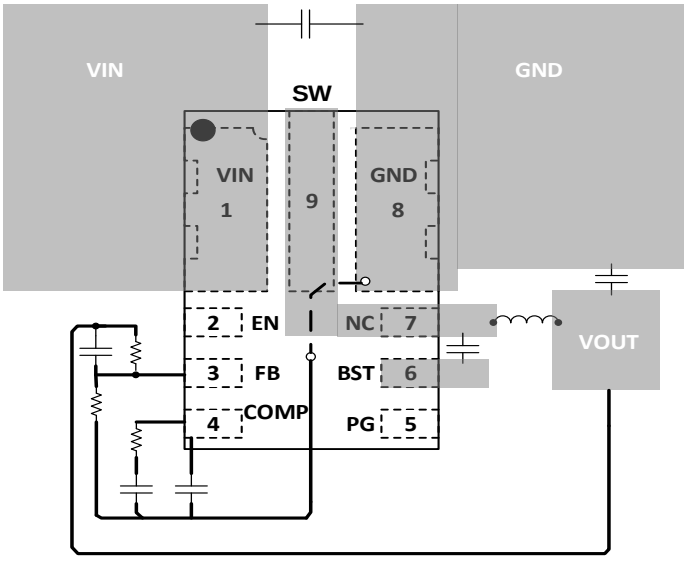
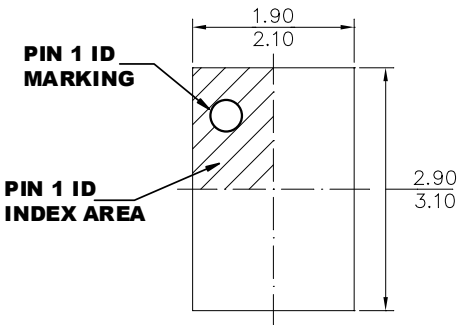
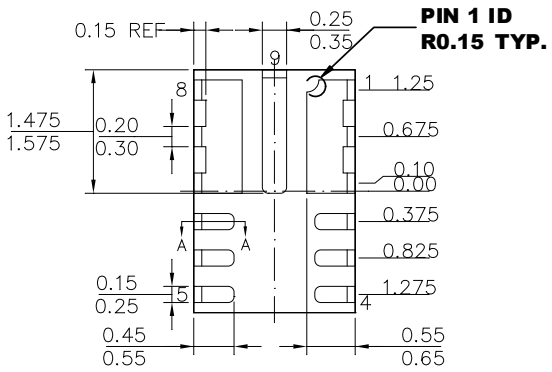


Figure 26. PCB Layout Example for application with external compensation

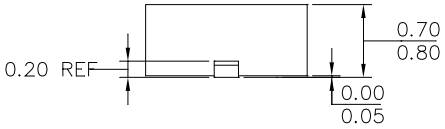
PACKAGE OUTLINE DRAWING FOR 9L FCQFN (2X3MM)
POD-0005 Revision 0.0



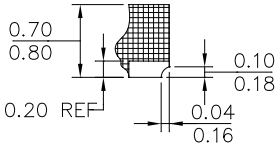
TOP VIEW



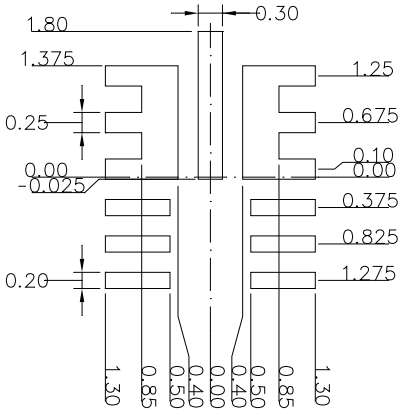
BOTTOM VIEW



SIDE VIEW



SECTION A-A

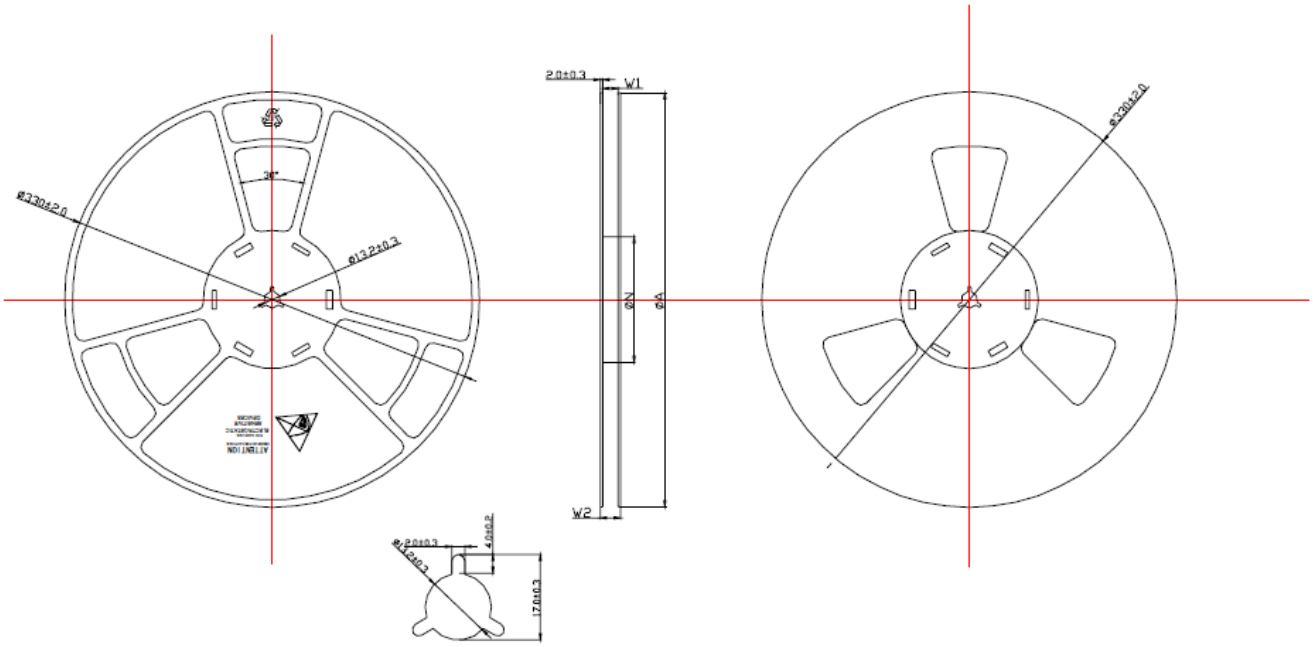


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

TAPE AND REEL INFORMATION



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	328	330	332
N	99	100	101
W1	12.4	-	-
W2	-	-	19.4