3.8V-36V Vin, 5A, High Efficiency Synchronous Step-down DCDC Converter with Adjustable Frequency

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Wide Input Range: 3.8V-36V
- Up to 5A Continuous Output Current
- 0.8V ±1% Feedback Reference Voltage
- Integrated 42mΩ High-Side and 18mΩ Low-Side Power MOSFETs
- Pulse Skipping Mode (PSM) with 25uA Quiescent Current in Sleep Mode
- 120ns Minimum On-time
- 5ms Internal Soft-start Time
- Adjustable Frequency 100kHz to 2.2MHz
- External Clock Synchronization
- Frequency Spread Spectrum (FSS) Modulation for EMI Reduction
- Precision Enable Threshold for adjustable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Low Dropout Mode Operation
- Derivable Inverting Voltage Regulator
- Over-voltage and Over-Temperature Protection
- Available in an ESOP-8L Package

APPLICATIONS

- Automotive System
- USB Type-C Power Delivery, USB Charging
- Industrial and Medical Distributed Power Supplies

DESCRIPTION

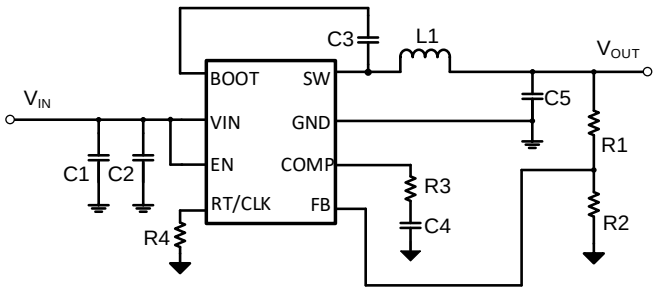
The SCT2450CQ is 5A synchronous buck converters with wide input voltage, ranging from 3.8V to 36V, which integrates a 42mΩ high-side MOSFET and a 18mΩ low-side MOSFET. The SCT2450CQ, adopting the peak current mode control, supports the Pulse Skipping Modulation (PSM) with typical 25uA low quiescent current which assists the converter on achieving high efficiency at light load or standby condition.

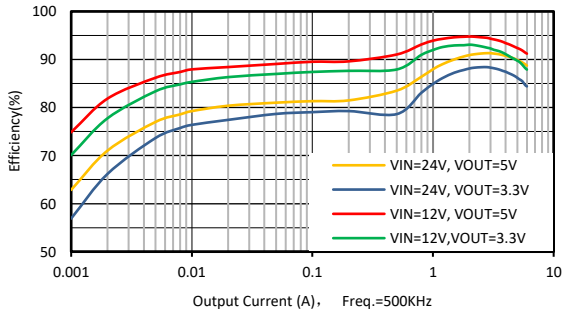
The SCT2450CQ features adjustable switching frequency from 100 kHz to 2.2 MHz with an external resistor, which provides the flexibility to optimize either efficiency or external component size. The converter supports external clock synchronization with a frequency band from 100kHz to 2.2MHz. The SCT2450CQ allows power conversion from high input voltage to low output voltage with a minimum 120ns on-time of high-side MOSFET.

The SCT2450CQ is an Electromagnetic Interference (EMI) friendly buck converter with implementing optimized design for EMI reduction. The SCT2450CQ features Frequency Spread Spectrum FSS with ±6% jittering span of the 500kHz switching frequency and modulation rate 1/512 of switching frequency to reduce the conducted EMI.

The SCT2450CQ offers cycle-by-cycle current limit and hiccup over current protection, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device is available in an 8-pin thermally enhanced ESOP-8L package.

TYPICAL APPLICATION





REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to production.

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT2450CQSTER	Tape & Reel	4000	450CQ	8	ESOP-8L	3

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted (1)

DESCRIPTION	MIN	MAX	UNIT
VIN (2)	-0.3	38	V
VIN Transient (300ms) (2)	-0.3	42	V
EN	-0.3	38	V
BOOT	-0.3	44	V
SW	-0.3	38	V
SW(<10ns) (3)	-3	38	V
BOOT-SW	-0.3	6	V
COMP, FB, RT/CLK	-0.3	6	V
Operating junction temperature TJ (4)	-40	150	°C
Storage temperature TSTG	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) The max VIN transient voltage is guaranteed by design and verified on bench.
(3) This applies to the ringing voltage generated by itself, not externally applied voltage.
(4) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN CONFIGURATION

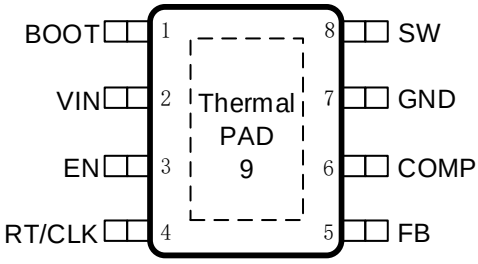


Figure 1. 8-Lead Plastic ESOP

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
BOOT	1	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when low-side power MOSFET is on or SW voltage is low.
VIN	2	Input supply voltage. Connect a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
EN	3	Enable pin to the regulator with internal pull-up current source. Pull below 1.1V to disable the converter. Float or connect to VIN to enable the converter. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold.
RT/CLK	4	Set the internal oscillator clock frequency or synchronize to an external clock. Connect a resistor from this pin to ground to set switching frequency. An external clock can be input directly to the RT/CLK pin. The internal oscillator synchronizes to the external clock frequency with PLL. If detected clocking edges stops, the operation mode automatically returns to resistor adjusted frequency.

FB	5	Inverting input of the trans-conductance error amplifier. The tap of external feedback resistor divider from the output to GND sets the output voltage. The device regulates FB voltage to the internal reference value of 0.8V typical.
COMP	6	Error amplifier output. Connect to frequency loop compensation network.
GND	7	Ground
SW	8	Regulator switching output. Connect SW to an external power inductor
Thermal Pad	9	Heat dissipation path of die. Electrically connection to GND pin. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.8	36	V
V_{OUT}	Output voltage range	0.8	36	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per AEC Q100-002(1)	-2	+2	kV
	Charged Device Model(CDM), per AEC-Q100-011	-1	+1	kV

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	ESOP-8L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	39.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.8	
Ψ_{JB}	Junction-to-board characterization parameter(1)	16.6	
$R_{\theta JCtop}$	Junction to case(top) thermal resistance(1)	57	
$R_{\theta JCbot}$	Junction to case(bottom) thermal resistance(1)	3.6	
$R_{\theta JB}$	Junction-to-board thermal resistance(1)	17.4	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2450CQ is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2450CQ. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual RθJA and RθJC.
(2) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN}=24V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		3.8		36	V
V_{IN_UVLO}	Input UVLO Threshold Hysteresis	V_{IN} rising		3.5 400	3.7	V mV
I_{SHDN}	Shutdown current from VIN pin	EN=0, no load		1	3	μA
I_Q	Quiescent current from VIN pin	EN floating, no load, non-switching, BOOT-SW=5V		25		μA
Power MOSFETs						
R_{DSON_H}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=5V		42		mΩ
R_{DSON_L}	Low-side MOSFET on-resistance			18		mΩ
Reference and Control Loop						
V_{REF}	Reference voltage of FB		0.792	0.8	0.808	V
G_{EA}	Error amplifier trans-conductance	-2μA<I_{COMP}<2μA, V_{COMP}=1V		300		μS
I_{COMP_SRC}	EA maximum source current	V_{FB}=V_{REF}-100mV, V_{COMP}=1V		30		μA
I_{COMP_SNK}	EA maximum sink current	V_{FB}=V_{REF}+100mV, V_{COMP}=1V		30		μA
V_{COMP_H}	COMP high clamp			3		V
V_{COMP_L}	COMP low clamp			0.4		V
Current Limit and Over Current Protection						
I_{LIM_HS}	High-side power MOSFET peak current limit threshold		6.8	8	9.2	A
I_{LIM_LSSRC}	Low-side power MOSFET souring current limit threshold			9		A
T_{HIC_W}	Over current protection hiccup wait time			512		cycles
T_{HIC_R}	Over current protection hiccup restart time			8192		cycles
Enable and Soft Startup						
V_{EN_H}	Enable high threshold			1.18	1.25	V
V_{EN_L}	Enable low threshold		1.03	1.1		V
I_{EN_L}	Enable pin pull-up current	EN=1V	1	1.5	2	μA
I_{EN_H}	Enable pin pull-up current	EN=1.5V		5.5		uA
T_{ss}	Internal soft start time			5		ms
Switching Frequency and External Clock Synchronization						
F_{RANGE_RT}	Frequency range using RT mode		100		2200	kHz
F_{SW}	Switching frequency	R_{RT}=200 kΩ(1%)	450	500	550	kHz
F_{RANGE_CLK}	Frequency range using CLK mode		100		2200	kHz
F_{JITTER}	Frequency spread spectrum in percentage of Fsw			±6		%
t_{ON_MIN}	Minimum on-time	V_{IN}=24V		120		ns
Protection						
V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} rising V_{FB}/V_{REF} falling		110 105		% %

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{BOOTUV}	BOOT-SW UVLO threshold	BOOT-SW falling Hysteresis		2.36 300		V mV
T_{SD}	Thermal shutdown threshold	T_J rising Hysteresis		170 25		°C °C

TYPICAL CHARACTERISTICS

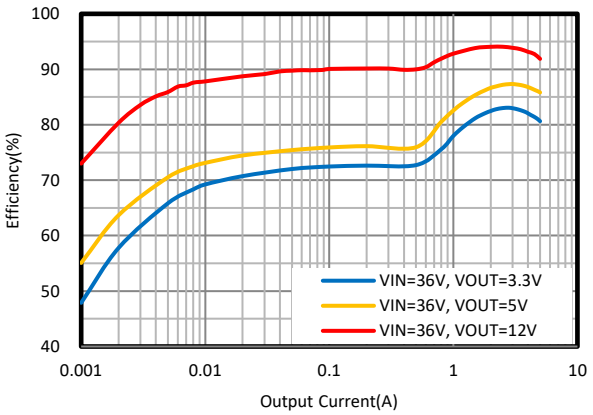


Figure 2. Efficiency vs Load Current, Vin=36V

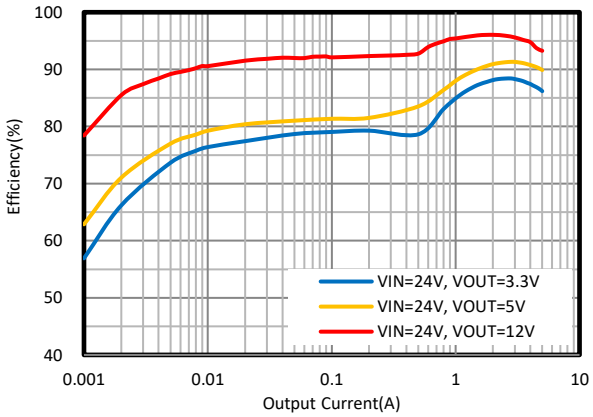


Figure 3. Efficiency vs Load Current, Vin=24V

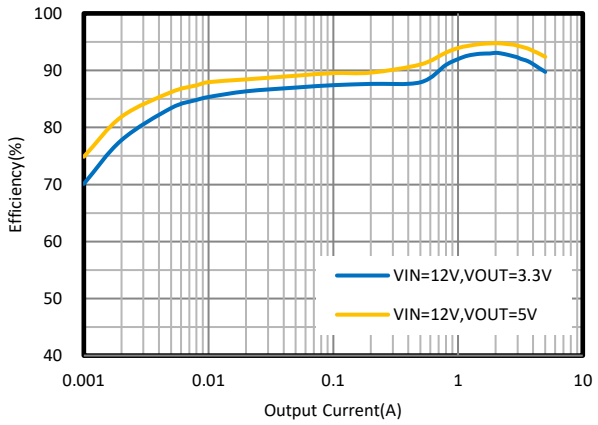


Figure 4. Efficiency vs Load Current, Vin=12V

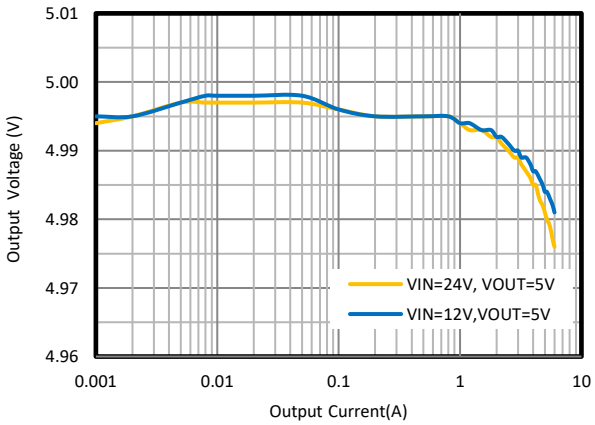


Figure 5. Load Regulation (Vout=5V)

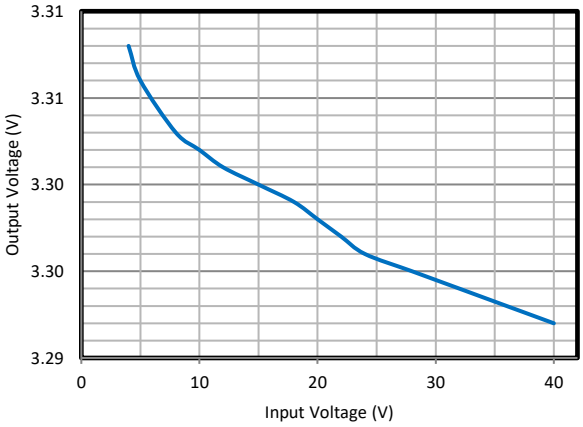


Figure 6. Line Regulation (Iout=5A)

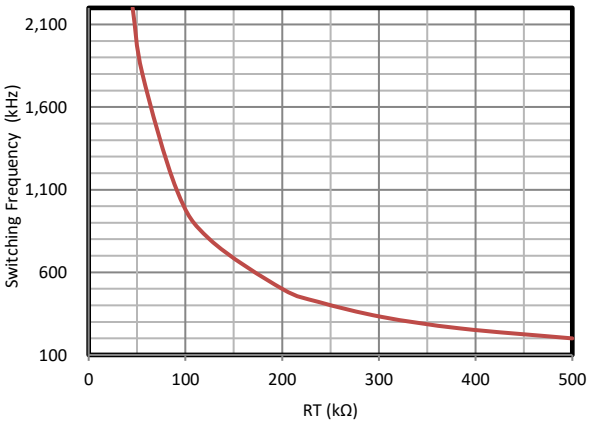


Figure 7.Clock Frequency vs RT/CLK Resistor

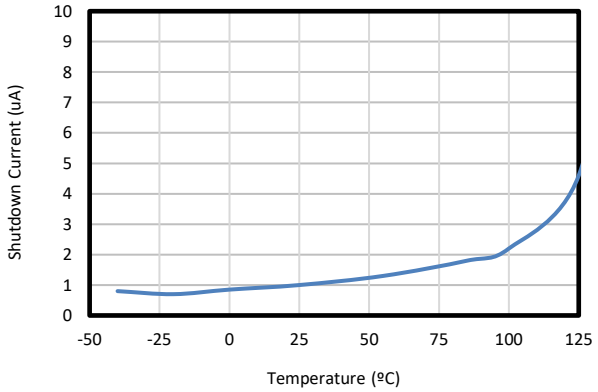


Figure 8. Shutdown Current vs Temperature

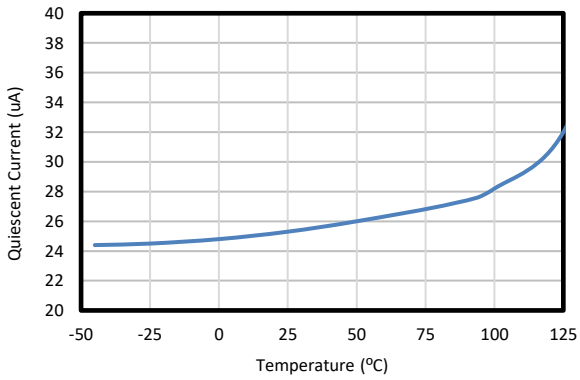


Figure 9. Quiescent Current vs Temperature

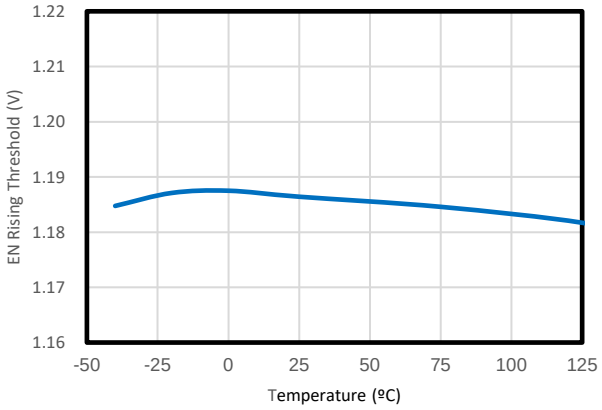


Figure 10. EN Threshold vs Temperature

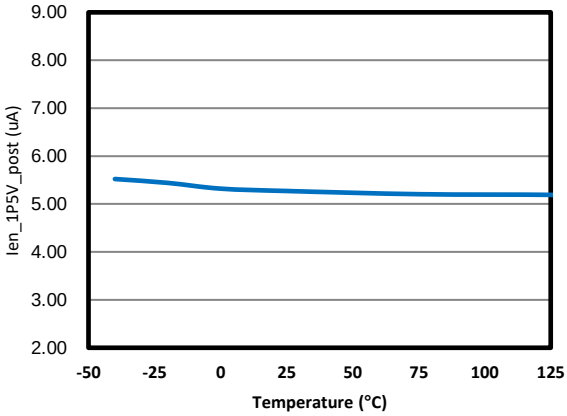


Figure 11. EN Pull-up Current vs Temperature

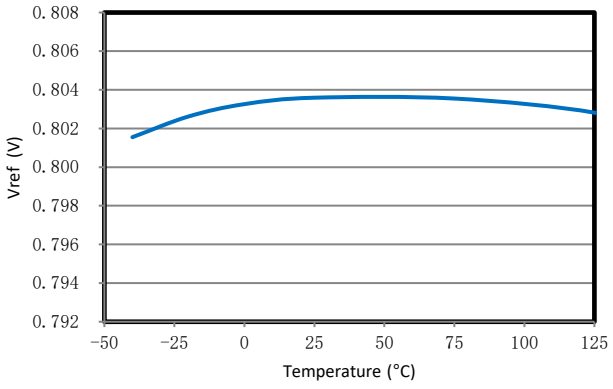


Figure 12. Reference Voltage vs Temperature

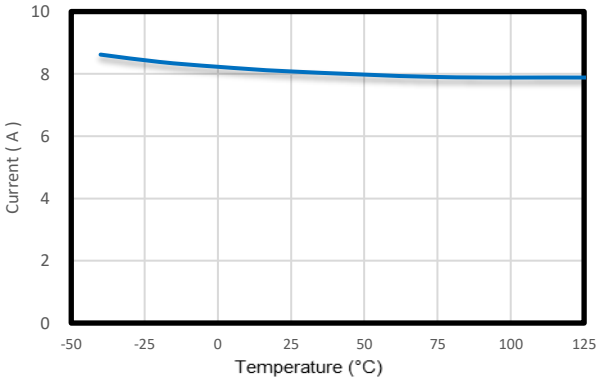


Figure 13. Peak Current Limit vs Temperature

FUNCTIONAL BLOCK DIAGRAM

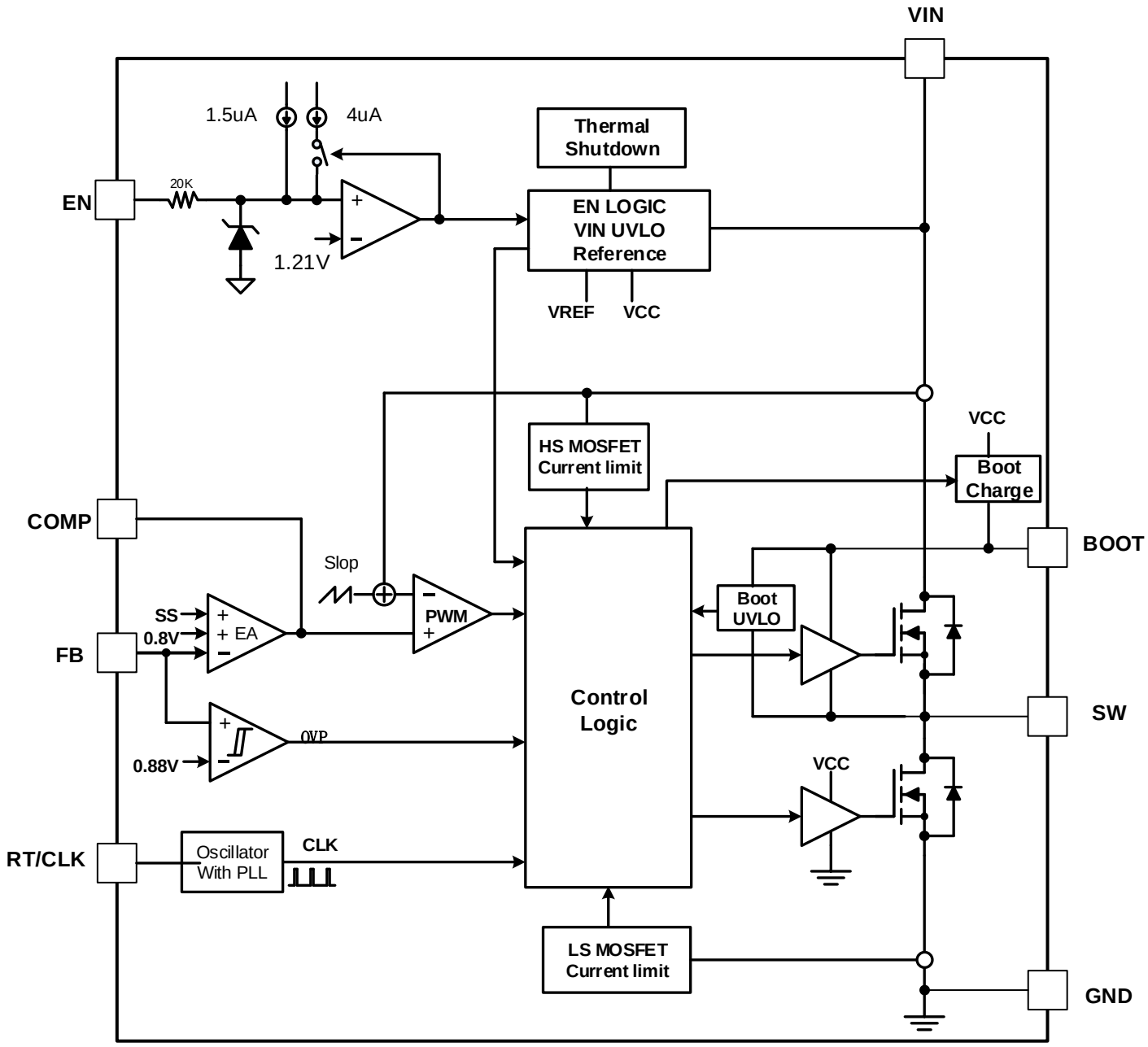


Figure 14. Functional Block Diagram

OPERATION

Overview

The SCT2450CQ is a 3.8V-36V input, 5A output, EMI friendly synchronous buck converter with built-in 42mΩ Rdson high-side and 18mΩ Rdson low-side power MOSFETs. It implements constant frequency peak current mode control to regulate output voltage, providing excellent line and load transient response and simplifying the external frequency compensation design.

The switching frequency is adjustable from 100kHz to 2.2MHz with two setting modes, resistor setting frequency mode and the clock synchronization mode, to optimizes either the power efficiency or the external components' sizes. The SCT2450CQ features an internal 5ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The device also supports monolithic startup with pre-biased output condition. The seamless mode-transition between PWM mode and PSM mode operations ensure high efficiency over wide load current range. The quiescent current is typically 25uA under no load or sleep mode condition to achieve high efficiency at light load.

The SCT2450CQ has a default input start-up voltage of 3.5V with 400mV hysteresis. The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN directly starts up the device automatically.

The SCT2450CQ implements the Frequency Spread Spectrum FSS modulation spreading of ±6% centered selected switching frequency. FSS improves EMI performance by not allowing emitted energy to stay in any one receiver band for a significant length of time.

The SCT2450CQ full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

Peak Current Mode Control

The SCT2450CQ employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the high-side MOSFET turns off. The synchronous low-side MOSFET Q2 turns on till the next clock cycle begins or the inductor current falls to zero.

The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The SCT2450CQ operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. When the load current decreases, an increment in the feedback voltage leads COMP voltage drop. When COMP falls to a low clamp threshold (400mV typically), device enters PSM. The output voltage decays due to output capacitor discharging during skipping period. Once FB voltage drops lower than the reference voltage, and the COMP voltage rises above low clamp threshold. Then high-side power MOSFET turns on in next clock pulse. After several switching cycles with typical 1A peak inductor current, COMP voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded.

This control scheme helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. The controller consumption quiescent current is 25uA during skipping period with no switching to improve efficiency further.

Enable and Under Voltage Lockout Threshold

The SCT2450CQ is enabled when the VIN pin voltage rises about 3.5V and the EN pin voltage exceeds the enable threshold of 1.18V. The device is disabled when the VIN pin voltage falls below 3.1V or when the EN pin voltage is

below 1.1V. An internal 1.5uA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 15 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$V_{rise} = 1.18 * \left(1 + \frac{R1}{R2}\right) - 1.5uA * R1 \quad (1)$$

$$V_{fall} = 1.1 * \left(1 + \frac{R1}{R2}\right) - 5.5uA * R1 \quad (2)$$

where

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO

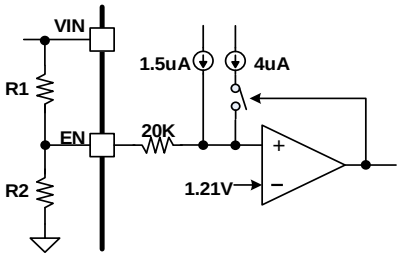


Figure 15. System UVLO by enable divide

Output Voltage

The SCT2450CQ regulates the internal reference voltage at 0.8V with ±1% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB\_BOT} \quad (3)$$

where

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Internal Soft-Start

The SCT2450CQ integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 0.8V reference voltage in 5ms. If the EN pin is pulled below 1.1V, switching stops and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

Switching Frequency and Clock Synchronization

The switching frequency of the SCT2450CQ is set by placing a resistor between RT/CLK pin and the ground, or synchronizing to an external clock.

In resistor setting frequency mode, a resistor placed between RT/CLK pin to the ground sets the switching frequency over a wide range from 100kHz to 2.2MHz. The RT/CLK pin voltage is typical 0.5V. RT/CLK pin is not allowed to be left floating or shorted to the ground. Use Equation 4 or the plot in Figure 16. to determine the resistance for a switching frequency needed.

$$RT(K\Omega) = \frac{100000}{fsw(KHz)} \quad (4)$$

where, fsw is switching clock frequency

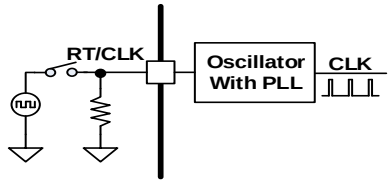


Figure 16. Setting Frequency and Clock Synchronization

In clock synchronization mode, the switching frequency synchronizes to an external clock applied to RT/CLK pin. The synchronization frequency range is from 100kHz to 2.2MHz and the rising edge of the SW synchronizes to the falling edge of the external clock at RT/CLK pin with typical 66ns time delay. A square wave clock signal to RT/CLK pin must have high level no lower than 2V, low level no higher than 0.4V, and pulse width larger than 80ns.

In applications where both resistor setting frequency mode and clock synchronization mode are needed, the device can be configured as shown in Figure 16. Before an external clock is present, the device works in resistor setting frequency mode. When an external clock presents, the device automatically transitions from resistor setting mode to external clock synchronization mode. An internal phase locked loop PLL locks internal clock frequency onto the external clock within typical 85us. The converter transitions from the clock synchronization mode to the resistor setting frequency mode when the external clock disappears.

Frequency Spread Spectrum

To reduce EMI, the SCT2450CQ implements Frequency Spread Spectrum (FSS). The FSS circuitry shifts the switching frequency of the regulator periodically within a certain frequency range around the adjusted switching frequency. The jittering span is ±6% of the switching frequency with 1/512 swing frequency. This frequency dithering function is effective for both frequency adjusted by resistor placed at RT/CLK pin and an external clock synchronization application.

Bootstrap Voltage Regulator and Low Drop-out Operation

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The UVLO of high-side MOSFET gate driver has rising threshold of 2.7V and hysteresis of 350mV. When the device operates with high duty cycle or extremely light load, bootstrap capacitor may be not recharged in considerable long time. The voltage at bootstrap capacitor is insufficient to drive high-side MOSFET fully on. When the voltage across bootstrap capacitor drops below 2.35V, BOOT UVLO occurs. The converter forces turning on low-side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee the converter's operation over a wide duty range.

During the condition of ultra-low voltage difference from the input to the output, SCT2450CQ operates in Low Drop-Out LDO mode. High-side MOSFET remains turning on as long as the BOOT pin to SW pin voltage is higher than BOOT UVLO threshold 2.7V. When the voltage from BOOT to SW drops below 2.4V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor periodically in the following several switching cycles. Low-side MOSFET only turns on for 100ns in each refresh cycle to minimize the output voltage ripple. Low-side MOSFET may turn on for several times till the bootstrap voltage is charged to higher than 2.7V for high-side MOSFET working normally. The effective duty cycle of the converter during LDO operation can be approaching to 100%

During slowing power up and power down application, the output voltage can closely track the input voltage ramping down thanks to LDO operation mode. As the input voltage is reduced to near the output voltage, i.e., during slowing power-up and power-down application, the off-time of the high side MOSFET starts to approach the minimum value. Without LDO operation mode, beyond this point the switching may become erratic and/or the output voltage will fall out of regulation. To avoid this problem the SCT2450CQ LDO mode automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation.

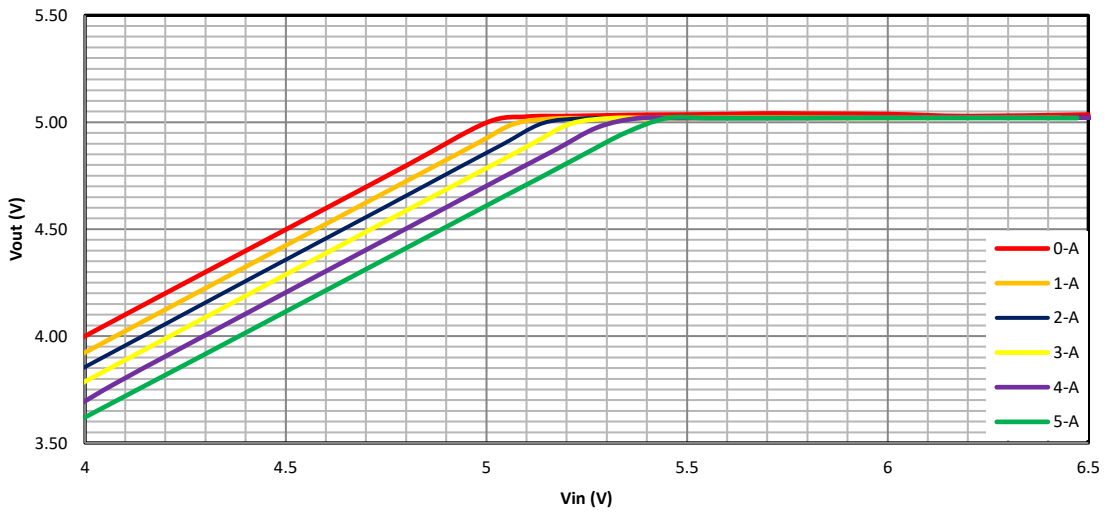


Figure 17. LDO Operation Characteristic (Vout =5V)

Over Current Limit and Hiccup Mode

The inductor current is monitored during high-side MOSFET Q1 and low-side MOSFET Q2 on. The SCT2450CQ implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition.

When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The COMP pin voltage ramps up to high clamp voltage 3.7V typical. When COMP voltage is clamped for 512 cycles, the converter stops switching. After remaining OFF for 8192 cycles，the device restarts from soft starting phase. If overload or hard short condition still exists during soft-start and make COMP voltage clamped at high for 512 cycles，the device enters into turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating operation.

The hiccup protection mode above makes the average short circuit current to alleviate thermal issues and protect the regulator.

Over voltage Protection

The SCT2450CQ implements the Over-voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 110% of internal 0.8V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase. When the FB pin voltage falls below 105% of the 0.8V reference voltage, the high-side MOSFET can turn on again.

Thermal Shutdown

The SCT2450CQ protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 170C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 145C, the device restarts with internal soft start phase.

APPLICATION INFORMATION

Typical Application

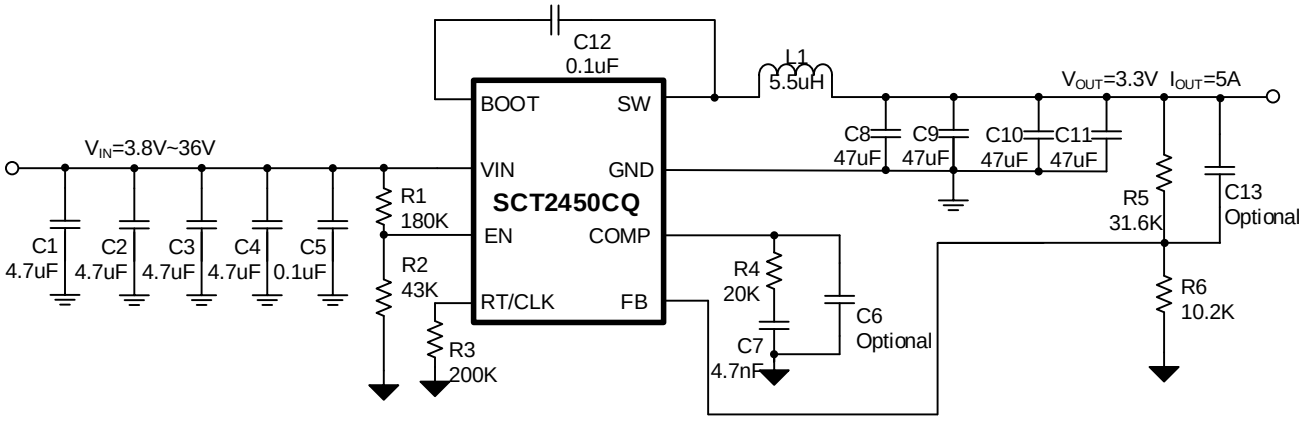


Figure 18. SCT2450CQ Design Example, 3.3V Output with Adjustable UVLO

Design Parameters

Design Parameters	Example Value
Input Voltage	24V Normal 3.8V to 36V
Output Voltage	3.3V
Maximum Output Current	5A
Switching Frequency	500 kHz
Output voltage ripple (peak to peak)	16.5mV
Transient Response 1.25A to 3.75A load step	ΔVout = 135mV
Start Input Voltage (rising VIN)	5.76V
Stop Input Voltage (falling VIN)	4.66V

Output Voltage

The output voltage is set by an external resistor divider R5 and R6 in typical application schematic. Recommended R6 resistance is 10.2KΩ. Use Equation 5 to calculate R5.

$$R_5 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_6 \quad (5)$$

where:

- V_{REF} is the feedback reference voltage, typical 0.8V

Table 1. R_5, R_6Value for Common Output Voltage (Room Temperature)

V_{OUT}	R_5	R_6
1.8 V	12.7 KΩ	10.2 KΩ
2.5 V	21.5 KΩ	10.2 KΩ
3.3 V	31.6 KΩ	10.2 KΩ
5 V	53.6 KΩ	10.2 KΩ
12 V	143 KΩ	10.2 KΩ
24V	294 KΩ	10.2 KΩ

Switching Frequency

Higher switching frequencies support smaller profiles of output inductors and output capacitors, resulting in lower voltage and current ripples. However, the higher switching frequency causes extra switching loss, which downgrads converter's overall power efficiency and thermal performance. The 120ns minimum on-time limitation also restricts the selection of higher switching frequency. In this design, a moderate switching frequency of 500 kHz is selected to achieve both small solution size and high efficiency operation.

The resistor connected from RT/CLK to GND sets switching frequency of the converter. The resistor value required for a desired frequency can be calculated using Equation 6, or determined from Figure 7.

$$R_3(\mathrm{K\Omega}) = \frac{100000}{\mathrm{fsw\ (kHz\ )}} \quad (6)$$

where:

- f_{SW} is the desired switching frequency

Table 2. R_{FSW} Value for Common Switching Frequencies (Room Temperature)

Fsw	R_3 (R_{FSW})
200 kHz	500 KΩ
330 kHz	301 KΩ
500 kHz	200 KΩ
1100 kHz	90.9 KΩ
2000 kHz	50 KΩ

Under Voltage Lock-Out

An external voltage divider network of R_1 from the input to EN pin and R_2 from EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 5.7V (start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 4.64 V (stop or disable). Use Equation 7 and Equation 8 to calculate the values 173 kΩ and 42 kΩ of R_1 and R_2 resistors.

$$\mathrm{V_{rise}} = 1.18 * \left(1 + \frac{R_1}{R_2}\right) - 1.5\mathrm{uA} * \mathrm{R_1} \quad (7)$$

$$\mathrm{V_{fall}} = 1.1 * \left(1 + \frac{R_1}{R_2}\right) - 5.5\mathrm{uA} * R_1 \quad (8)$$

Inductor Selection

There are several factors should be conQITsidered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance(DCR). Larger inductance results in less inductor current ripple and therefore leads

to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 9.

$$I_{LPP} = \frac{V_{OUT}*(V_{IN}-V_{OUT})}{V_{IN}*L*f_{SW}} \quad (9)$$

Where

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 10 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW}*LIR*I_{OUT(max)}} * (1 - \frac{V_{OUT}}{V_{IN(max)}}) \quad (10)$$

Where

- L_{MIN} is the minimum inductance required
- f_{sw} is the switching frequency
- V_{OUT} is the output voltage
- $V_{IN(max)}$ is the maximum input voltage
- $I_{OUT(max)}$ is the maximum DC load current
- LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in Equation 11 and Equation 12.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (11)$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \quad (12)$$

Where

- I_{LPEAK} is the inductor peak current
- I_{OUT} is the DC load current
- I_{LPP} is the inductor peak-to-peak current
- I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 8A. The most conservative approach is to choose an inductor with a saturation current rating greater than 8A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT2450CQ can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a higher maximum output current.

For this design, use LIR=0.2 or 0.3, and the inductor value is calculated to be 5uH, the RMS inductor current is 6A and the peak inductor current is 7.2A. The chosen inductor is a WE 744325550, which has a saturation current rating of 12A and a RMS current rating of 10A. This also has a typical inductance of 5.5μH at no load and 4.7 μH at 6A load. The inductor DCR is 10.3 mΩ.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 13.

$$I_{CINRMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \quad (13)$$

The worst case condition occurs at V_{IN}=2*V_{OUT}, where:

$$I_{CINRMS} = 0.5 * I_{OUT} \quad (14)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increases.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 15 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

For this example, three 4.7μF, X7R ceramic capacitors rated for 50 V in parallel are used. And a 0.1 μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 16 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * f_{SW}^2 * L * C_{OUT} * V_{IN}} \quad (16)$$

Where

- $\Delta V_{OUT}$is the output voltage ripple
- f_{SW} is the switching frequency
- L is the inductance of inductor
- C_{OUT} is the output capacitance
- V_{OUT} is the output voltage

- $V_{IN}$is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 47μF ceramic output capacitors work for most applications.

Compensation Components

The SCT2450CQ employs peak current mode control for easy compensation and fast transient response. An external network comprising resister R4, ceramic capacitors C7 and optional C6 connected to the COMP pin is used for the loop compensation. The Equation17 shows the close-loop small signal transfer function.

$$H(S)=\left[A_{EA}*\frac{1+\frac{S}{2\pi*f_{Z1}}}{\left(1+\frac{S}{2\pi*f_{P1}}\right)*\left(1+\frac{S}{2\pi*f_{P3}}\right)}\right]*\left[G_{ISNS}*\frac{V_{OUT}}{I_{OUT}}*\frac{1+\frac{S}{2\pi*f_{Z2}}}{1+\frac{S}{2\pi*f_{P2}}}\right]*\frac{V_{FB}}{V_{OUT}} \quad (17)$$

where

- A_{EA} is error amplifier voltage gain
- G_{ISNS} is COMP to SW current trans-conductance, 11.2A/V typically

The DC voltage gain of the loop is given by Equation 18.

$$A_{VDC}=A_{EA}*G_{ISNS}*\frac{V_{FB}}{I_{OUT}} \quad (18)$$

The system has two noteworthy poles: one is due to the compensation capacitor C7 and the error amplifier output resistor. The other is caused by the output capacitor and the load resistor. These poles as located at:

$$f_{P1}=\frac{1}{2\pi*R_{OEA}*C_7}=\frac{G_{EA}}{2\pi*A_{EA}*C_7} \quad (19)$$

$$f_{P2}=\frac{1}{2\pi*R_{LOAD}*C_{OUT}}=\frac{I_{OUT}}{2\pi*V_{OUT}*C_{OUT}} \quad (20)$$

where

- R_{OEA} is error amplifier output resistor
- G_{EA} is Error amplifier trans-conductance, 300uS typically
- R_{LOAD} is equivalent load resistor

The system has one zero of importance from R4 and C7. fz1 is used to counteract the fp2, and fz1 located at:

$$f_{Z1}=\frac{1}{2\pi*C_7*R_4} \quad (21)$$

The system may have another important zero if the output capacitor has a large capacitance or a high ESR value. The zero, due to the ESR and the capacitance of the output capacitor is calculated by Equation 22.

$$f_{Z2}=\frac{1}{2\pi*C_{OUT}*ESR} \quad (22)$$

In this case, a third pole set by the optional compensation capacitor C6 and the compensation resistor R4 is used to compensates the effect of the ESR zero. This pole is calculated by Equation 23.

$$f_{P3}=\frac{1}{2\pi*C_6*R_4} \quad (23)$$

The crossover frequency of converter is shown in Equation 24.

$$f_C=\frac{V_{FB}}{V_{OUT}}*\frac{G_{EA}*G_{ISNS}*R_4}{2\pi*C_{OUT}} \quad (24)$$

The system crossover frequency, where the feedback loop has unity gain, is important. A lower crossover frequency results in slower line and load transient response. A higher crossover frequency could cause the system unstable. A recommended rule of thumb is to set the crossover frequency to be approximately 1/10 of switching frequency.

The following steps can be followed to calculate the external compensation components. Calculate the compensation resistor R4 with Equation 25 once crossover frequency is selected.

$$R_4 = \frac{V_{OUT}}{V_{FB}} * \frac{2\pi * C_{OUT} * f_C}{G_{EA} * G_{ISNS}} \quad (25)$$

Then calculate C7 by placing a compensation zero at or before the output stage pole.

$$C_7 = \frac{R_{LOAD} * C_{OUT}}{R4} \quad (26)$$

Determine if the optional compensation capacitor C6 is required. Generally, it is required if the ESR zero f_{Z2} is located less than half of the switching frequency. Then fp3 can be used to cancel fz2. C6 can be calculated with Equation 27.

$$C_6 = \frac{C_{OUT} \times ESR}{R_4} \quad (27)$$

Table 3 lists typical values of compensation components for some standard output voltages with various output ceramic capacitors and inductors. The values of the compensation components have been optimized for fast transient responses and good stability. For the conditions not list in Table 3, customers can use Equation 25-Equation 27 to optimize the compensation components.

Table 3: Compensation Values for Typical Output Voltage/Capacitor Combinations at fsw=500kHz

Vout	L1	COUT	R4	C7	C6
1.8V	3.3uH	4*47uF	12.1K	6.8nF	100pF(optional)
2.5V	4.7uH	4*47uF	16.9K	4.7nF	68pF (optional)
3.3V	5.5uH	4*47uF	20K	4.7 nF	47pF (optional)
5V	7.8uH	4*47uF	33.2K	3.3nF	22pF (optional)
12V	10uH	4*47uF	53.6K	1nF	220pF

Application Waveforms

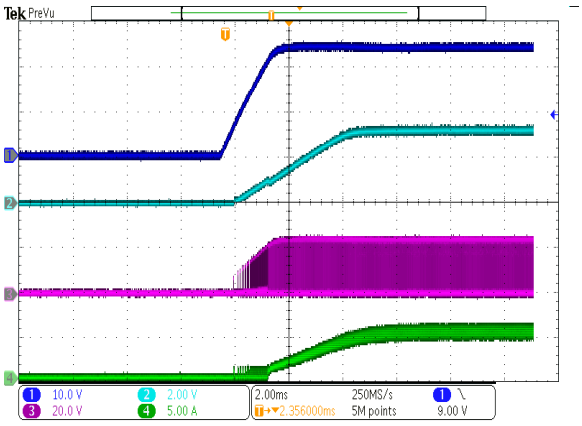


Figure 19. Power up

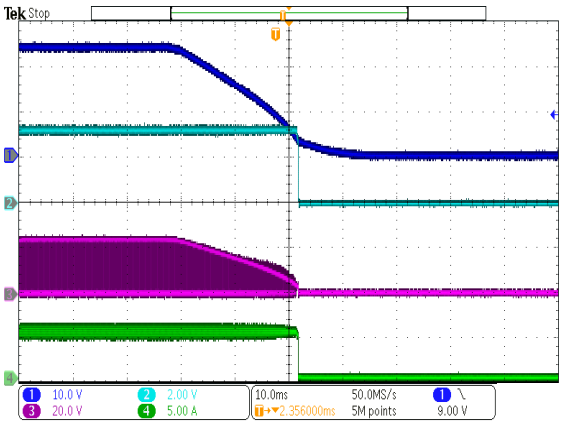


Figure 20. Power down

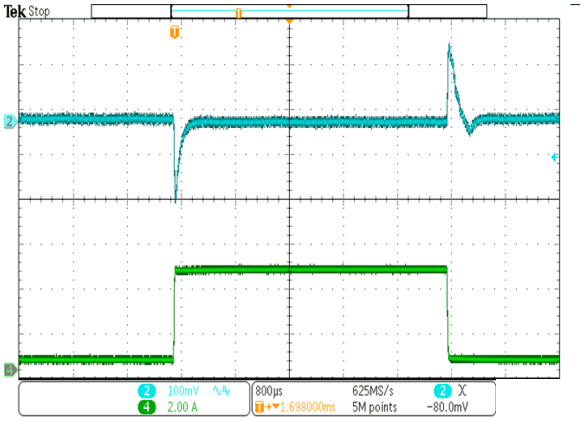


Figure 21. Load Transient (0.5A-4.5A, 250mA/us)

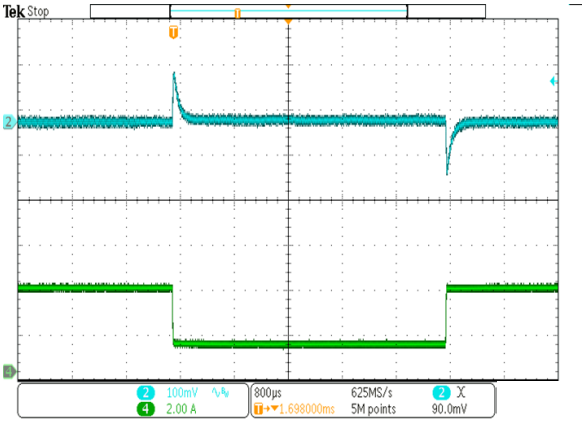


Figure 22. Load Transient (1.25A-3.75A, 250mA/us)

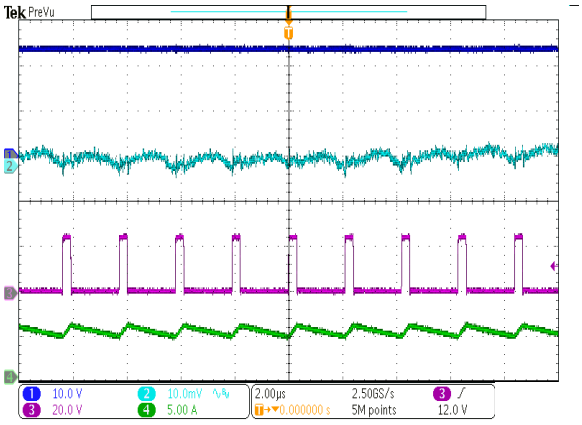


Figure 23. SW and Vout Ripple

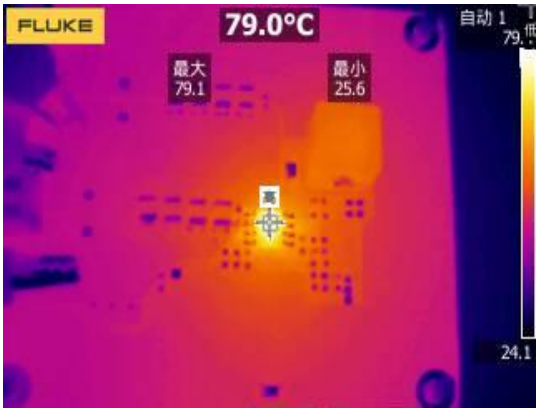


Figure 24. Thermal, 3.3Vout/5A

Layout Guideline

Proper PCB layout is a critical for SCT2450CQ's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing overheat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias directly under the IC. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias underneath the thermal pad. Improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. it is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
5. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
6. The RT/CLK terminal is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace.
7. UVLO adjust and RT resistors, loop compensation and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
8. Route BOOT capacitor trace on the other layer than top layer to provide wide path for topside ground.
9. For achieving better thermal performance, a four-layer layout is strongly recommended.

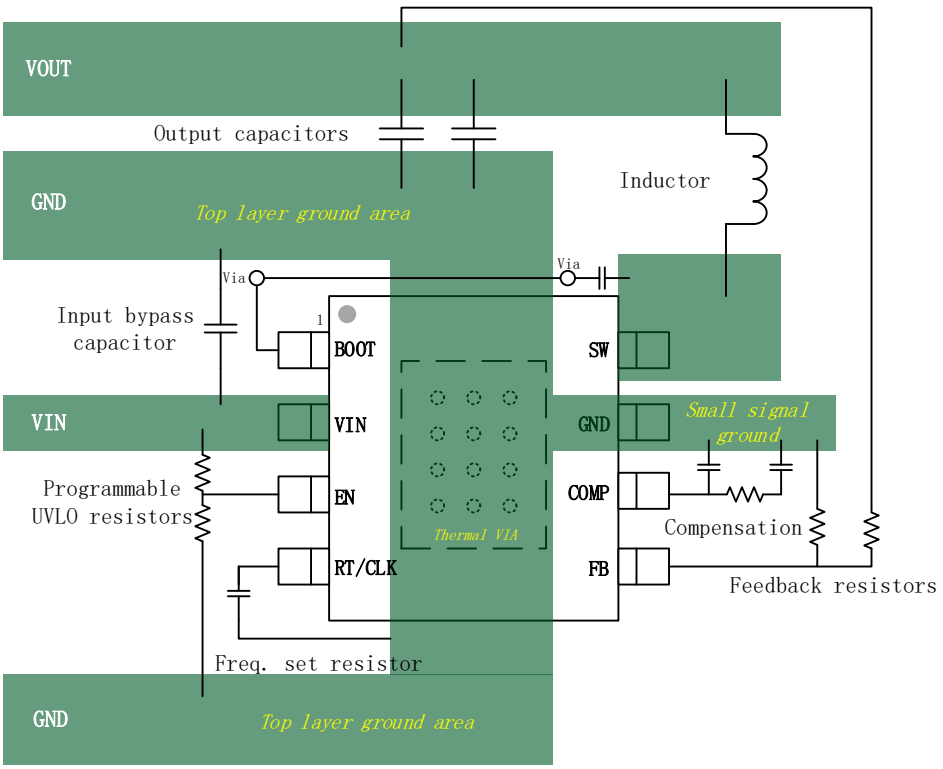
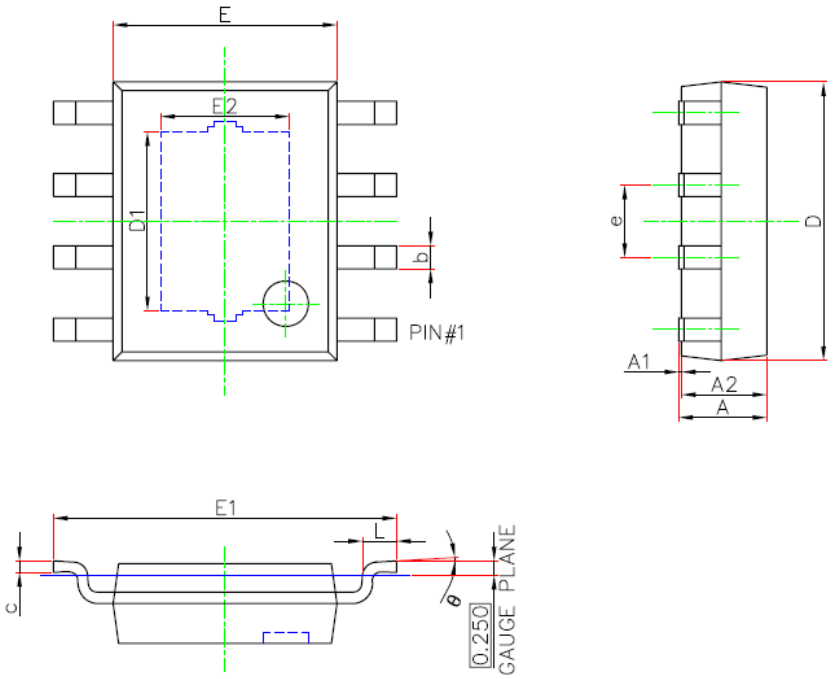


Figure 25. PCB Layout Example

PACKAGE INFORMATION



ESOP-8L (95x130) Package Outline Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.050	3.250	0.120	0.128
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.160	2.360	0.085	0.093
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

TAPE AND REEL INFORMATION